Design Example Report

Title	***45 W Flyback Converter with Lossless Zero Crossing Circuit Using LinkSwitch™-HP LNK6777E and CAPZero-2™ CAP200DG***
Specification	90 VAC – 265 VAC Input; 19 V, 2.37 A Output
Application	Appliance
Author	Applications Engineering Department
Document Number	DER-581
Date	February 7, 2017
Revision	1.1

Summary and Features

- Highly energy efficient
  - 88% full load and active mode efficiency
  - Meets DoE 6 efficiency requirements (end of cable)
  - <60 mW no-load consumption at 230 VAC input
  - Multimode operation maximizes efficiency over full load range
- Use of optocoupler feedback with LinkSwitch-HP devices
  - Enhanced output regulation and transient response
- Lossless generation of zero crossing signal
  - Reduces no-load input power and generates isolated zero crossing signal
- Extensive protection features including OVP, OTP, brown-in/out, line overvoltage, and lost-regulation (auto-restart)
- Meets EN-550022 and CISPR-22 Class B conducted/radiated EMI with 6 dB margin.
- Meets IEC61000-4-5, 3 kV / 3 kV surge.

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5245 Hellyer Avenue, San Jose, CA 95138 USA.

Tel: +1 408 414 9200 Fax: +1 408 414 9201

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This report describes a universal input, 19 V, 45 W isolated flyback converter employing LNK6777E from the LinkSwitch-HP family of ICs. It contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer, along with test data and waveform plots of the most important electrical waveforms.

The most significant aspect of this design is to demonstrate implementing secondary side optocoupler feedback with LinkSwitch-HP devices.

Typical LinkSwitch-HP designs are primary side regulated however the addition of optocoupler feedback allows the part to address applications with both stringent transient response (0 to 100%) and no-load input power (<75 mW) requirements.

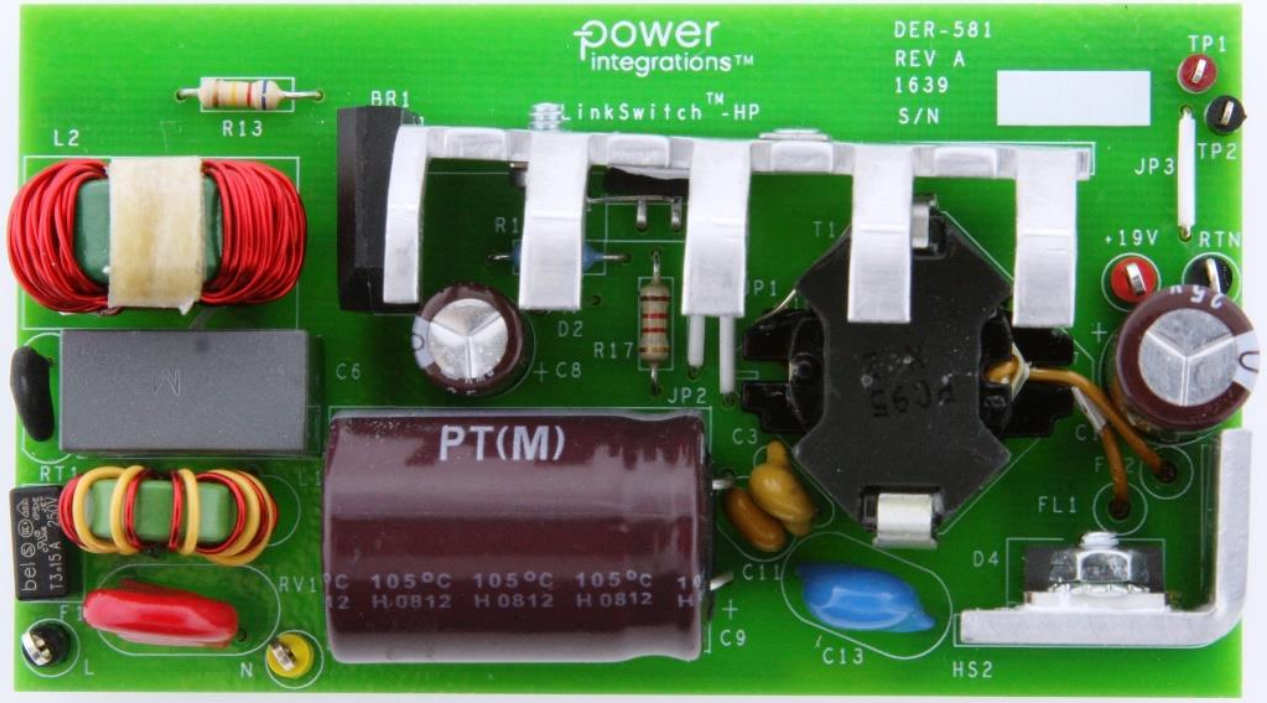

Figure 1 – Prototype Top View.

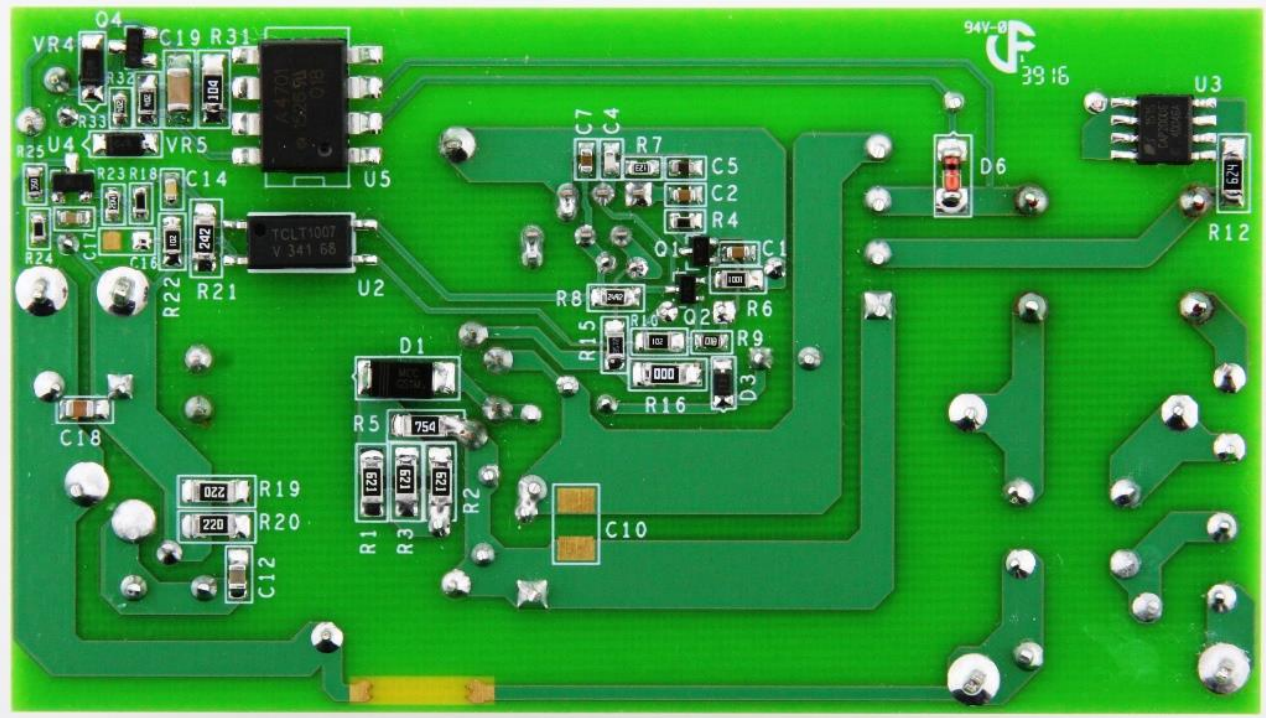

Figure 2 – Prototype Bottom View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-Load Input Power	P_{NL}			75	mW	230 VAC.
Output						
Output Voltage	V_{OUT}	18.05	19	19.95	V	±5%
Output Ripple Voltage	V_{RIPPLE}			150	mVpp	20 MHz Bandwidth, $V_{IN(MIN)}$, $I_{OUT(MAX)}$.
Output Current	I_{OUT}	0.0		2.37	A	
Total Output Power						
Continuous Output Power	P_{OUT}	0		45	W	
Efficiency						
Full Load Efficiency	η	86			%	90 VAC and Full Load.
Environmental						
Conducted EMI		Meets EN55022B				6 dB Margin.
Safety		Designed to meet IEC950, UL1950 Class II				
Surge	**DM**	3			kV	1.2/50 μs surge, IEC 61000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
	CM	3				
ESD	**Air**	-16.5		16.5	kV	Air Discharge onto Output Connector.
	Contact	-8.8		8.8	kV	Contact Discharge onto Output Connector.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

3 Schematic

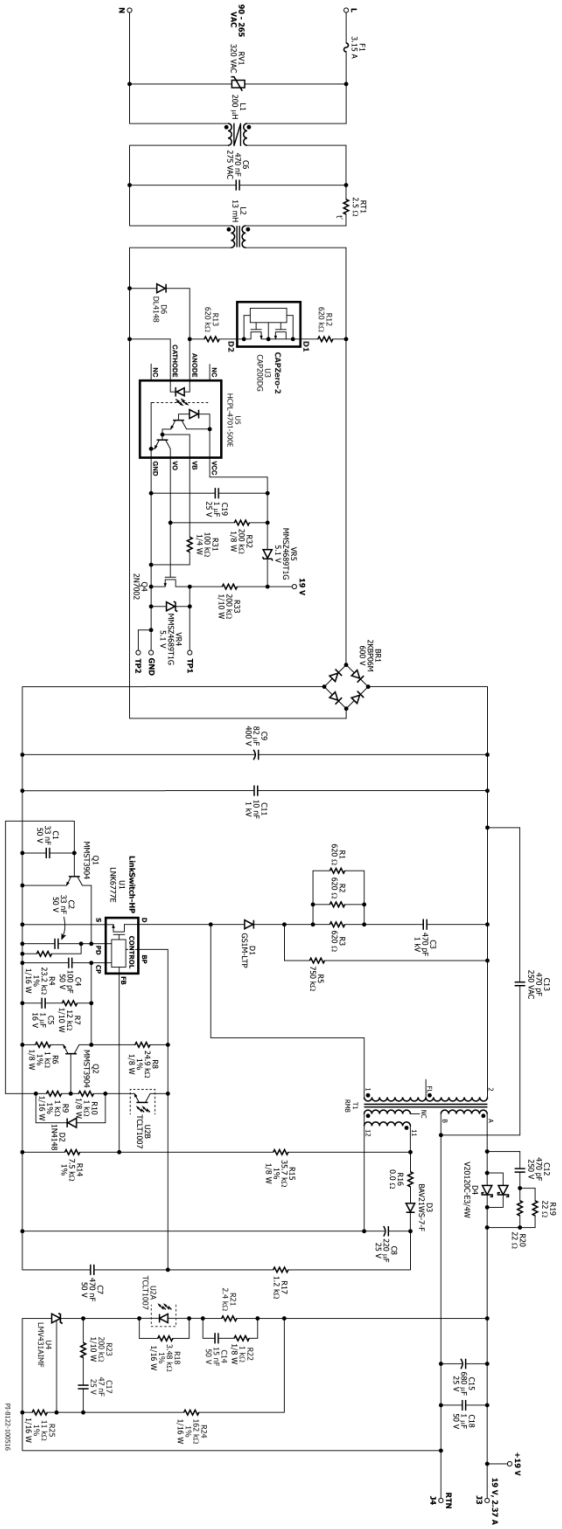

Figure 3 – Schematic.

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4 Circuit Description

The circuit shown in Figure 3 utilizes the LNK6777E device in a 19 V, 45 W isolated flyback power supply.

4.1 *Input Rectification and Filtering*

Fuse F1 provides overcurrent protection to the circuit and isolates it from the AC supply in the event of a fault. Diode bridge BR1 rectifies the AC input. Capacitor C6, in conjunction with inductors L1 and L2, constitute the EMI filter for attenuating both common mode and differential mode conducted noise.

NTC thermistor RT1 limits inrush current of the supply when line voltage is first applied.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

4.2 *CAPZero-2 and Zero Crossing Detection*

Resistors R12 and R13 in addition to CAPZero-2 are provided to discharge the EMI filter capacitors after input supply is disconnected from the circuit. While the AC line is present, CAPZero-2 minimizes the no-load input power consumption.

The CAPZero-2 IC is also used for zero cross detection of AC input voltage while benefiting from lower no load consumption. Circuit comprising D6, U5, VR4, VR5, R31, R32, R33, C1 and Q4 is used in addition to CAPZero-2 IC to obtain zero crossing signal of AC input voltage.

When the AC line voltage is positive with respect to neutral, optocoupler photo diode of U5 conducts and drives the photo transistor which causes collector voltage to be low and when the AC line is negative with respect to neutral, the optocoupler photo diode of U5 is reverse biased and turns off the photo transistor. Capacitor C19 was used as a decoupling capacitor to the optocoupler V_{CC}.

Zener diode VR5 is used to limit the maximum voltage supplied to the optocoupler U5 V_{CC}. Optocoupler U5 drives FET Q4. Rectangular signal at drain of Q4 is logic level high when line voltage is higher than the neutral and logic level low when the line voltage is lower than the neutral. Resistor R33 and Zener diode VR4 ensure that the drain voltage of Q4 is TTL compatible.

4.3 *LinkSwitch-HP Primary*

The schematic in Figure 3 depicts a 19 V, 45 W LinkSwitch-HP based flyback converter implemented using the LNK6777E IC. The LNK6777E device (U1) integrates an oscillator, an error amplifier and multi-mode control circuit, start-up and protection circuitry and a high-voltage power MOSFET all in one monolithic IC.

One side of the power transformer is connected to the high-voltage bus and the other side is connected to the DRAIN (D) pin of U1. At the start of a switching cycle, the controller turns the power MOSFET on and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the limit threshold which is set by the output of internal error amplifier (COMPENSATION (CP) pin voltage), the controller turns the power

MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitors.

Capacitor C7 (470 nF) connected to the BYPASS (BP) pin sets overvoltage protection (OVP) and over-temperature protection (OTP) to latching and lost regulation protection to automatic restart attempts (auto-restart) after a given off-period (typ. 1500 ms).

4.4 *Primary RCD Clamp*

Diode D1, C3, R1, R2, R3 and R5 form a RCD snubber that is used to limit the voltage stress across the LinkSwitch-HP. Peak drain voltage is therefore limited to typically less than 640 V at 265 VAC – providing significant margin to the 725 V drain voltage rating (BV_{DSS}).

4.5 *Output Rectification*

Output rectification of the 19 V output is provided by diode D4 and filtering is provided by capacitor C15, C18. The snubber formed by R19, R20 and C12 provides high frequency filtering for improved EMI.

4.6 *External Current Limit Setting-*

The maximum cycle-by-cycle current limit is set by the resistor R4 connected to the PROGRAM (PD) pin. A 23.2 kΩ resistor in the design sets the maximum current limit to 60% of the LNK6777E IC's default current limit.

4.7 *Feedback and Compensation Network*

Secondary side regulation was used for this design instead of primary side regulation to achieve both low no-load consumption (<100 mW) and transient response requirements (±5%).

The basic approach is to use an optocoupler to directly drive the CP pin of the LinkSwitch-HP IC. The CP voltage can be considered to be the internal error voltage and therefore changing the error voltage directly changes the power processed by the device (primary current and switching frequency).

4.7.1 Primary Side Regulation

In a standard LinkSwitch-HP design the output voltage is determined through the coupling between the bias and secondary windings, with the voltage on the bias winding being regulated.

The voltage on the bias winding is sensed via a resistor divider and connected to the FB pin of the IC. The voltage sensed at the FB pin produces a control voltage at the CP pin. This control voltage determines the operating peak primary current and the operating switching frequency. Resistor R7 and capacitors C4 and C5 are used for control loop compensation.

Due to the addition of secondary side feedback the bias winding no longer provides regulation under normal operation. However for the approach to work the bias winding feedback set point must be set above the secondary feedback set point. Therefore the R14 and R15 resistor divider ratio is set such that the FB pin is slightly (~10%) below its 2 V reference voltage when the output voltage is in regulation.

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This allows the secondary side feedback to dominate, i.e. as the output voltage tries to exceed the level set by the secondary side feedback the optocoupler will conduct and the control loop will close.

One side benefit of this is that there are effectively two regulation loops such that if the secondary loop is defeated due to a fault (i.e. open optocoupler), then the power supply will regulate from the primary side at the slightly higher output voltage (~10%).

The primary winding sense cannot be simply removed when using optocoupler feedback as the divider R14 and R15 is used to indirectly monitor the bus voltage during the integrated power MOSFET on-time to provide line undervoltage and overvoltage functions.

4.7.2 Secondary Side Regulation

The output voltage is controlled using shunt regulator U4. Resistors R24 and R25 sense the output voltage, forming a resistor divider connected to the reference input of IC U4. Changes in the output voltage and hence the voltage at the reference input of U4 results in changes in the cathode voltage of IC U4 and therefore optocoupler U2 LED current.

This changes the voltage on CP pin of U1 (via Q2) and therefore the operating peak primary current and the operating switching frequency to maintain output voltage regulation.

Diode D2 is used to clamp the voltage from optocoupler emitter to ground in order to avoid overdriving of Q2 (maximum voltage on the optocoupler emitter will be the V_F of D2 plus the V_{BE} of Q1).

If D2 is not used, during a load transient from full load to no-load (output voltage exceeds the regulation set point) U2B transistor is saturated and voltage at the U2B emitter rises to >6 V. This then over drives Q2 causing the voltage at Q2 emitter higher level and in turn raises the CP pin voltage. Raising the CP pin causes increased power delivery and the output voltage goes further out of regulation, essentially latching the condition.

Resistor R6 and R9 sets a gain of 1 along with Q2 and Q1 and voltage across R6 will be approximately 300 mV at no-load. This is well below the minimum voltage on the CP pin at no load.

Resistors R21, R22, R23, and capacitors C14, C17 are used for control loop compensation.

The primary side of the optocoupler feedback circuit consists of Q1, Q2, R6, R7, R8, R9, R10, D2, C4, C5 and U2.

Since the FB pin divider network is set to deliver higher output voltage than the actual regulated output (set by optocoupler feedback) a lost regulation fault is falsely detected by the IC (the FB pin voltage never reaches the 2 V regulation threshold).

To prevent the false fault detection causing the part to enter auto-restart a workaround is implemented using Q1. Current only flows in the optocoupler when the control loop is closed and the output is in regulation. The optocoupler current is therefore used to drive the base of Q1, which pulls down the PD pin of the LinkSwitch-HP device, inhibiting the part from entering auto-restart (by preventing the 128 cycles of the PD pin between VPD(DL) (0.5 V_{TYP}) and VPD(DU) (1.2 V_{TYP}))

This arrangement still allows the programming functions on the PD pin to be detected at start-up as Q1 is off and also allows auto-restart in the event of output overload or short circuit as again Q1 will be off.

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5 PCB Layout

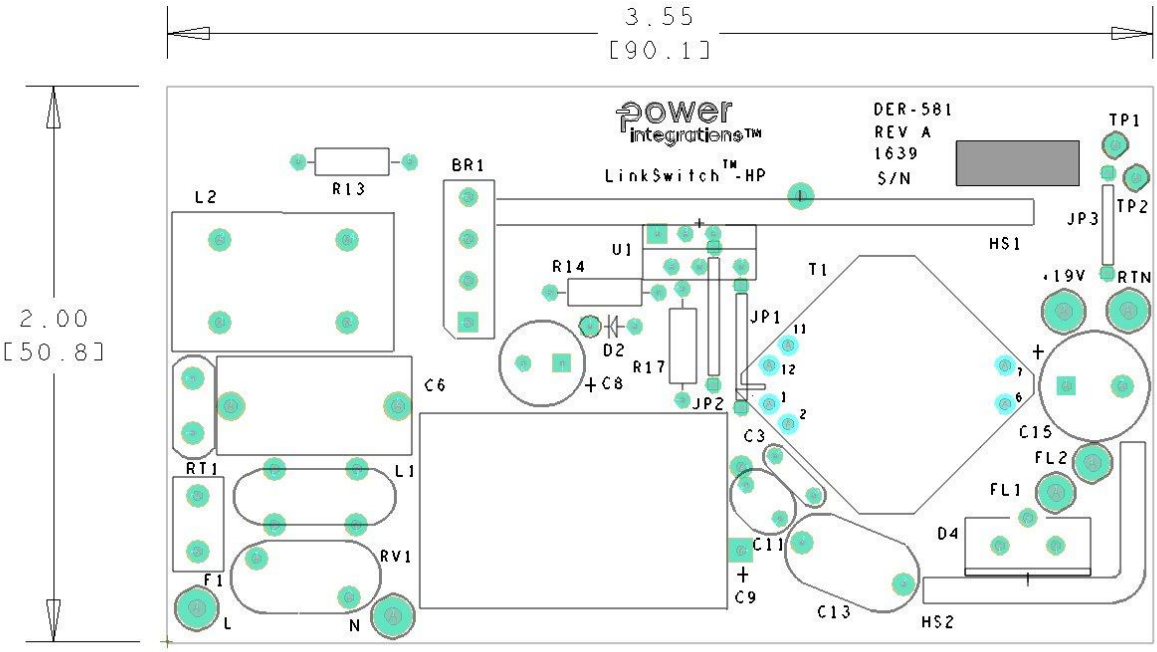

Figure 4 – PCB Top Side.

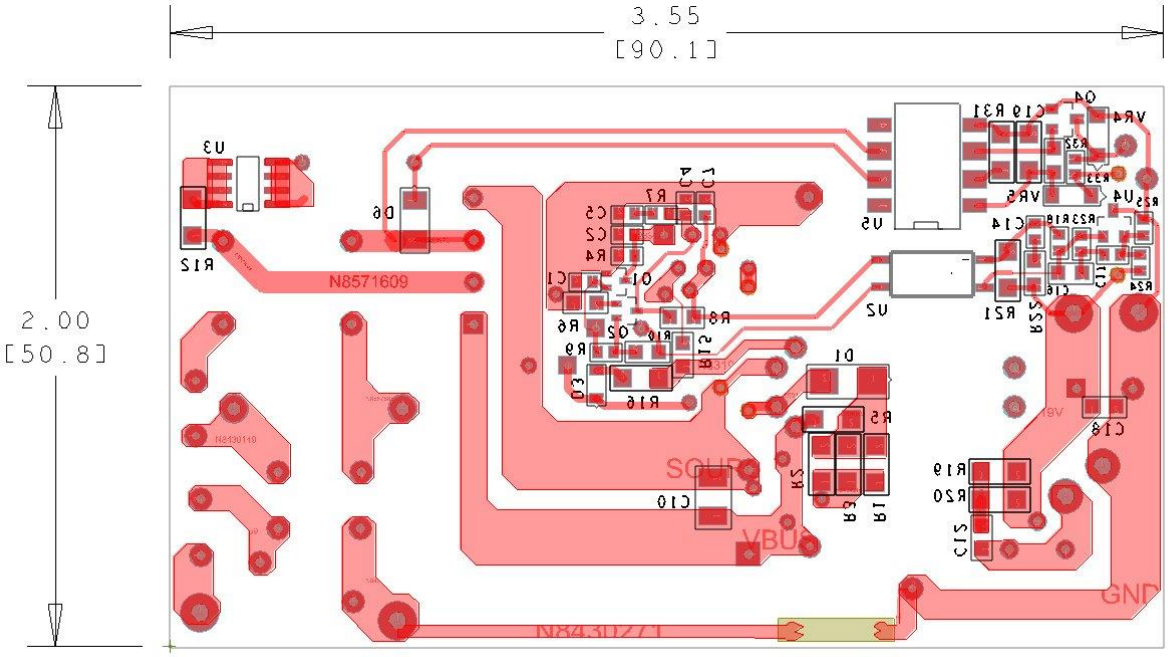

Figure 5 – PCB Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	+19V	Test Point, RED,THRU-HOLE MOUNT	5010	Keystone
2	1	BR1	600 V, 2 A, Bridge Rectifier, Glass Passivated	2KBP06M-E4/51	Vishay
3	2	C1 C2	33 nF 50 V, Ceramic, X7R, 0603	GRM188R71H333KA61D	Murata
4	1	C3	470 pF, 1 kV, Disc Ceramic	NCD471K1KVY5FF	NIC
5	1	C4	100 pF 50 V, Ceramic, NPO, 0603	CC0603JRNPO9BN101	Yageo
6	1	C5	1 μF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
7	1	C6	470 nF, 275 VAC, Film, X2	80-R46KI347050P1M	Kemet
8	1	C7	470 nF, 50 V, Ceramic, X7R, 0603	UMK107B7474KA-TR	Taiyo Yuden
9	1	C8	220 μF, 25 V, Electrolytic, Gen. Purpose, (8 x 11.5)	EKMG250ELL221MHB5D	Nippon Chemi-Con
10	1	C9	82 μF, 400 V, Electrolytic, (18 x 25)	20-00831-00	Nichicon
11	1	C11	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX
12	1	C12	470 pF, 250 V, Ceramic, GCM, 0805	GCM21A7U2E471JX01D	Murata
13	1	C13	470 pF, 250 VAC, Film, X1Y1	CD95-B2GA471KYNS	TDK
14	1	C14	15 nF, 50 V, Ceramic, X7R, 0603	CL10B153KB8NFNC	Samsung
15	1	C15	680 μF, 25 V, Electrolytic, Very Low ESR, 23 mΩ, (10 x 20)	EKZE250ELL681MJ20S	Nippon Chemi-Con
16	1	C17	47 nF 25 V, Ceramic, X7R, 0603	CC0603KRX7R8BB473	Yago
17	1	C18	1 μF,50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
18	1	C19	1 μF, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK
19	1	D1	1000 V, 1 A, DO-214AC	GS1M-LTP	Micro Commercial
20	1	D2	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
21	1	D3	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
22	1	D4	120 V, 10 A, Schottky, TO-220AB	V20120C-E3/4W	Vishay
23	1	D6	75 V, 0.15 A, Fast Switching, 4 ns, MELF, SOD80C	DL4148-TP	Micro Commercial
24	1	ESIP CLIP1	Heat Sink Hardware, Edge Clip, 12.40 mm x 6.50 mm	TRK-24	Kang Tang
25	1	F1	3.15 A, 250V, Slow, RST	507-1181	Belfuse
26	2	FL1 FL2	PCB Terminal Hole, 18 AWG	N/A	N/A
27	2	GREASE1 GREASE2	Thermal Grease, Silicone, 5 oz Tube	CT40-5	ITW Chemtronics
28	1	HS1	FAB, HEATSINK, eSIP, DER453		Custom
29	1	HS2	FAB, HEATSINK, DIODE, DER453		Custom
30	2	JP1 JP2	Wire Jumper, Insulated, 24 AWG, 0.5 in	C2003A-12-02	Gen Cable
31	1	JP3	Wire Jumper, Insulated, 24 AWG, 0.4 in	C2003A-12-02	Gen Cable
32	2	L RTN	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
33	1	L1	200 μH, Common mode choke, 12 X 6 X 4	TSD-3908	Premier Magnetics
34	1	L2	13 mH, Common Mode Choke	TSD-3909	Premier Magnetics
35	1	N	Test Point, YEL,THRU-HOLE MOUNT	5014	Keystone
36	1	NUT1	Nut, Hex, Kep 4-40, S ZN Cr3 plateing RoHS	4CKNTZR	Any RoHS Compliant Mfg.
37	2	Q1 Q2	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3904-7-F	Diodes, Inc.
38	1	Q4	60V, 115MA, SOT23-3	2N7002-7-F	Diodes, Inc.
39	3	R1 R2 R3	RES, 620 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ621V	Panasonic
40	1	R4	RES, 23.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2322V	Panasonic
41	1	R5	RES, 750 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ754V	Panasonic
42	1	R6	RES, 1.00 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1001V	Panasonic
43	1	R7	RES, 12 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ123V	Panasonic
44	1	R8	RES, 24.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2492V	Panasonic
45	1	R9	RES, 1 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1001V	Panasonic
46	2	R10 R22	RES, 1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
47	1	R12	RES, 620 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ624V	Panasonic
48	1	R13	RES, 620 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-620K	Yageo

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49	1	R14	RES, 7.5 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-7K50	Yageo
50	1	R15	RES, 35.7 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3572V	Panasonic
51	1	R16	RES, 0 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEY0R00V	Panasonic
52	1	R17	RES, 1.2 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-1K2	Yageo
53	1	R18	RES, 3.48 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3481V	Panasonic
54	2	R19 R20	RES, 22 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ220V	Panasonic
55	1	R21	RES, 2.4 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ242V	Panasonic
56	2	R23 R33	RES, 200 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ204V	Panasonic
57	1	R24	RES, 162 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1623V	Panasonic
58	1	R25	RES, 11 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1102V	Panasonic
59	1	R31	RES, 100 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ104V	Panasonic
60	1	R32	RES, 200 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ204V	Panasonic
61	1	RT1	NTC Thermistor, 2.5 Ω, 3 A	SL08 2R503	Ametherm
62	1	RV1	320 VAC, 48 J, 10 mm, RADIAL	V320LA10P	Littlefuse
63	1	SCREW1	SCREW MACHINE PHIL 4-40X 3/16 SS	67413609	MSC Industrial
64	1	SCREW2	SCREW MACHINE PHIL Flat head 4-40 X 5/16 SS		Any RoHS Compliant Mfg.
65	1	T1	Bobbin, RM8, Vertical, 12 pins Transformer	BRM08-1112CP-W-P5.0 PNK-67771T	MH&W International Premier Magnetics
66	1	TP1	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
67	1	TP2	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
68	1	U1	LinkSwitch-HP, eSIP-7F	LNK6777E	Power Integrations
69	1	U2	OPTOISOLATOR, 5KV, TRANSISTOR, 4-SOP	TCLT1007	Vishay
70	1	U3	CAPZero-2, SO-8C	CAP200DG	Power Integrations
71	1	U4	1.24V Shunt Regulator IC, 1%, -40 to 85 C, SOT23-3	LMV431AIMF	National Semi
72	1	U5	Optocoupler, 5.00 kV, High Speed, DIP-8 Gull Wing	HCPL-4701-500E	Broadcom / Avago
73	2	VR4 VR5	5.1 V, 5%, 500 mW, SOD-123, -55 C ~ +150 C	MMSZ4689T1G	ON Semi
74	1	WASHER1	WASHER FLAT #4 Zinc, OD 0.219, ID 0.125, Thk 0.032, Yellow Chromate Finish	5205820-2	Tyco

7 Transformer Design Spreadsheet

ACDC_LinkSwitch-HP_101714; Rev.2.0; Copyright Power Integrations 2014	INPUT	OUTPUT	UNIT	ACDC_LinkSwitchHP_101714 Rev 2-0.xls: LinkSwitch-HP Flyback Continuous/Discontinuous Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES				
VACMIN	90	90	V	Minimum AC Input Voltage
VACMAX	265	265	V	Maximum AC Input Voltage
fL		50	Hz	AC Mains Frequency
VO	19	19	V	Output Voltage (main)
PO	45	45	W	Load Power
n	0.90	0.90		Efficiency Estimate
Z		0.50		Loss Allocation Factor
VB	10	10	V	Bias Voltage
tC		3	ms	Bridge Rectifier Conduction Time Estimate
CIN	82	82	uF	Input Filter Capacitor
Package	**E/V**	E/V		E and V Package Selected
Enclosure	**Open Frame**	Open Frame		Open Frame type enclosure
Heatsink	**Metal**	Metal		Metallic heatsink thermally connected to the exposed metal on the E-package
ENTER LinkSwitch-HP VARIABLES				
LinkSwitch-HP	**LNK6777E**	**LNK6777E**		Manual Device Selection
ILIMITMIN		2.418	A	Minimum Current limit
ILIMITMAX		2.782	A	Maximum current limit
ILIMITMIN_EXT		1.451	A	External Minimum Current limit
ILIMITMAX_EXT		1.669	A	External Maximum current limit
KI	**0.6**	0.600		Current limit reduction factor
Rpd		23.20	k-ohm	Program delay Resistor
Cpd		33.00	nF	Program delay Capacitor
Total programmed delay		0.18	sec	Total program delay
fS		132	kHz	LinkSwitch-HP Switching Frequency
fSmin		120	kHz	LinkSwitch-HP Minimum Switching Frequency
fSmax		136	kHz	LinkSwitch-HP Maximum Switching Frequency
KP	0.53	0.53		Ripple to Peak Current Ratio (0.4 < KP < 6.0)
VOR	130.00	130.00	V	Reflected Output Voltage
Voltage Sense				
VUVON		96.30	V	Undervoltage turn on
VUVOFF		39.25	V	Undervoltage turn off
VOV		433.44	V	Overvoltage threshold
FMAX_FULL_LOAD		126.72	kHz	Maximum switching frequency at full load
FMIN_FULL_LOAD		111.81	kHz	Minimum switching frequency at full load
TSAMPLE_FULL_LOAD		2.92	us	Minimum available Diode conduction time at full load. This should be greater than 2.5 us
TSAMPLE_LIGHT_LOAD		1.83	us	Minimum available Diode conduction time at light load. This should be greater than 1.4 us
VDS		1.71	V	LinkSwitch-HP on-state Drain to Source Voltage.
VD	0.70	0.70	V	Output Winding Diode Forward Voltage Drop
VDB		0.70	V	Bias Winding Diode Forward Voltage Drop
FEEDBACK SENSING SECTION				
RFB1		30.90	k-ohms	Feedback divider upper resistor
RFB2		7.15	k-ohms	Feedback divider lowerr resistor
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				

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Select Core Size	**RM8/I**	RM8/I		Manual Core Selected
Core		RM8/I		Selected Core
Custom Core				Enter name of custom core is applicable
AE		0.63	cm^2	Core Effective Cross Sectional Area
LE		3.84	cm	Core Effective Path Length
AL		3000	nH/T^2	Ungapped Core Effective Inductance
BW		8.6	mm	Bobbin Physical Winding Width
M		0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2	2		Number of Primary Layers
NS	8	8		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS				
VMIN		88	V	Minimum DC Input Voltage
VMAX		375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.60		Maximum Duty Cycle
IAVG		0.57	A	Average Primary Current
IP		1.29	A	Peak Primary Current
IR		0.68	A	Primary Ripple Current
IRMS		0.75	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP_TYP		690	uH	Typical Primary Inductance
LP_TOL	5	5	%	Primary inductance Tolerance
NP		53		Primary Winding Number of Turns
NB		4		Bias Winding Number of Turns
ALG		247	nH/T^2	Gapped Core Effective Inductance
BM		2675	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP		3634	Gauss	Peak Flux Density (BP<3700)
BAC		709	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		1455		Relative Permeability of Ungapped Core
LG		0.29	mm	Gap Length (Lg > 0.1 mm)
BWE		17.2	mm	Effective Bobbin Width
OD	0.40	0.40	mm	Maximum Primary Wire Diameter including insulation
INS		0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.34	mm	Bare conductor diameter
AWG		28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		161	Cmils	Bare conductor effective area in circular mils
CMA		215	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Lumped parameters				
ISP		8.51	A	Peak Secondary Current
ISRMS		4.03	A	Secondary RMS Current
IO		2.37	A	Power Supply Output Current
IRIPPLE		3.26	A	Output Capacitor RMS Ripple Current
CMS		806	Cmils	Secondary Bare Conductor minimum circular mils
AWGS		21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS		0.73	mm	Secondary Minimum Bare Conductor Diameter
ODS		1.08	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS		0.17	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS				
VDRAIN		668	V	Peak voltage acoss drain to source of Linkswitch-HP
PIVS		76	V	Output Rectifier Maximum Peak Inverse Voltage
PIVB		41	V	Bias Rectifier Maximum Peak Inverse Voltage
1st output				
VO1		19.00	V	Output Voltage
IO1		2.37	A	Output DC Current

PO1		45.00	W	Output Power
VD1		0.7	V	Output Diode Forward Voltage Drop
NS1		8.00		Output Winding Number of Turns
ISRMS1		4.031	A	Output Winding RMS Current
IRIPPLE1		3.26	A	Output Capacitor RMS Ripple Current
PIVS1		76	V	Output Rectifier Maximum Peak Inverse Voltage
CMS1		806	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1		21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1		0.73	mm	Minimum Bare Conductor Diameter
ODS1		1.08	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output				
VO2		0.00	V	Output Voltage
IO2		0.00	A	Output DC Current
PO2		0.00	W	Output Power
VD2		0.7	V	Output Diode Forward Voltage Drop
NS2		0.28		Output Winding Number of Turns
ISRMS2		0.000	A	Output Winding RMS Current
IRIPPLE2		0.00	A	Output Capacitor RMS Ripple Current
PIVS2		2	V	Output Rectifier Maximum Peak Inverse Voltage
CMS2		0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2		N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2		N/A	mm	Minimum Bare Conductor Diameter
ODS2		N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output				
VO3		0.00	V	Output Voltage
IO3		0.00	A	Output DC Current
PO3		0.00	W	Output Power
VD3		0.7	V	Output Diode Forward Voltage Drop
NS3		0.28		Output Winding Number of Turns
ISRMS3		0.000	A	Output Winding RMS Current
IRIPPLE3		0.00	A	Output Capacitor RMS Ripple Current
PIVS3		2	V	Output Rectifier Maximum Peak Inverse Voltage
CMS3		0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3		N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3		N/A	mm	Minimum Bare Conductor Diameter
ODS3		N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power		45	W	Total Power for Multi-output section
Negative Output	N/A	N/A		If negative output exists enter Output number; eg: If VO2 is negative output, select 2

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8 Magnetics

8.1 *Transformer T1 Specification*

8.1.1 Electrical Diagram

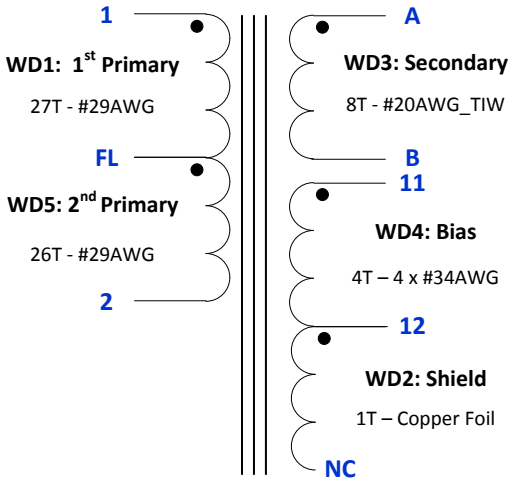

Figure 6 – Transformer Electrical Diagram.

8.1.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1, 2, 11, 12 to fly leads A-B.	3000 VAC
Primary Inductance	Pins 1-2, all others open, measured at 100 kHz, 0.4 V_{RMS}.	690 µH, ±5%
Resonant Frequency	Pins 1-2, all others open.	1700 kHz (Min.)
Primary Leakage	Pins 1-2, with A-B shorted, measured at 100 KHz, 0.4 V_{RMS}.	7.0 µH (Max.)

8.1.3 Material List

Item	Description
[1]	Core: RM8, TDK-PC95, gapped for ALG of 285nH/T².
[2]	Bobbin: RM8, Vertical, 12 pins(6/6), TDK; or equivalent.
[3]	Clip: RM8: Allstar Magnetic, PN: CLI/P-RM8/I.
[4]	Magnet wire: #29 AWG Double Coated, Solderable.
[5]	Magnet wire: #34 AWG Double Coated, Solderable.
[6]	Magnet wire: #20 AWG Triple Insulated Wire.
[7]	Copper Shield: Use copper foil 1 mil thick, 8.5 mm wide, 35.0 mm long, and covered with tape, see Figure 3 below and illustration below for constructing.
[8]	Tape: 3M 1298 Polyester Film, 1 mil thick, 9.0 mm wide.
[9]	Bus bare wire: #26 AWG, Belden Electronics Division.
[10]	Varnish.

8.1.4 Transformer Build Diagram

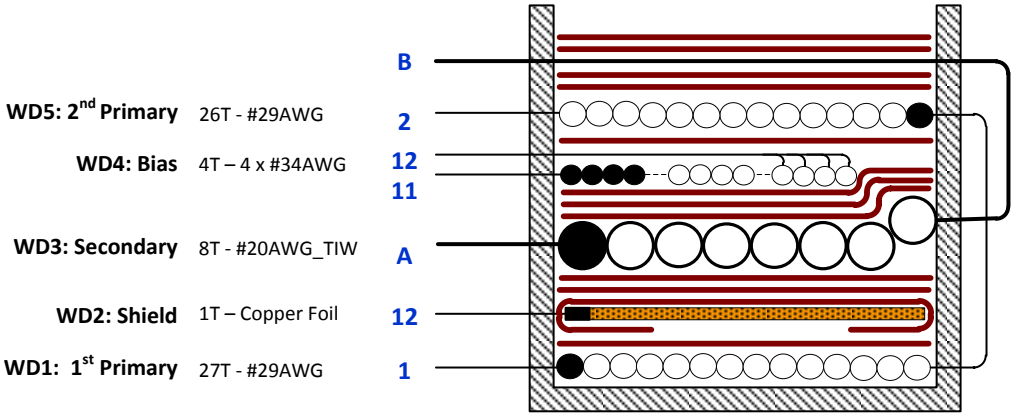

Figure 7 – Transformer Build Diagram.

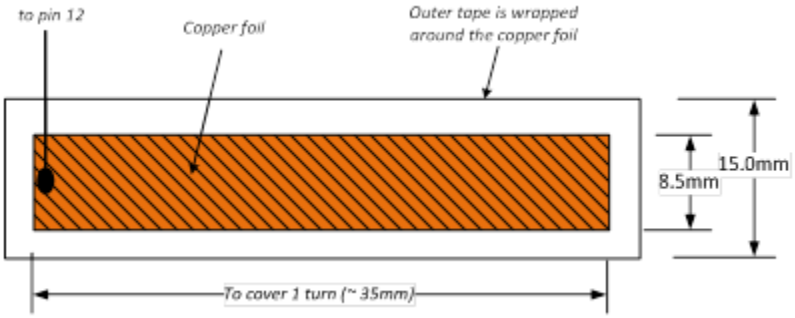

Figure 8 – Copper Shield.

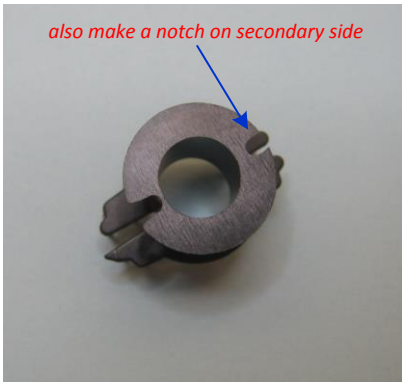

Figure 9 – Bobbin Notch.

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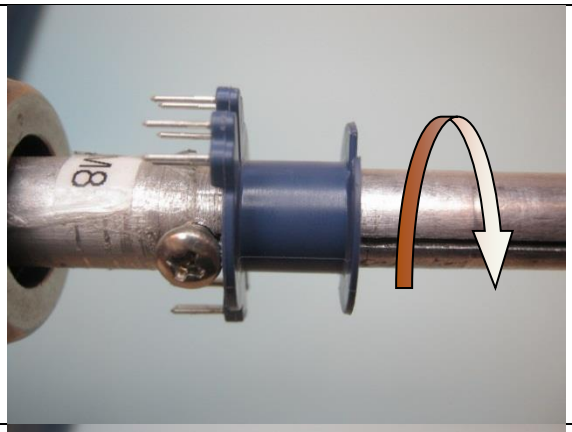
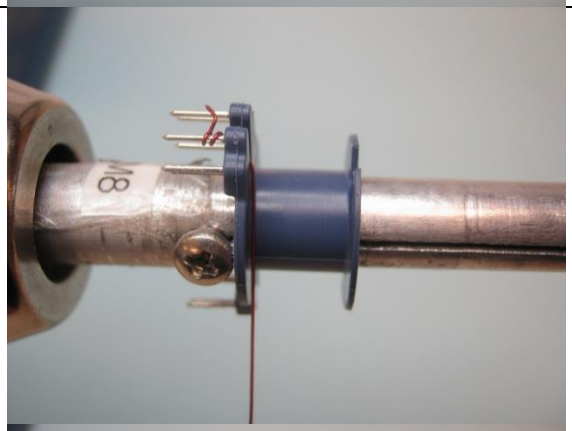
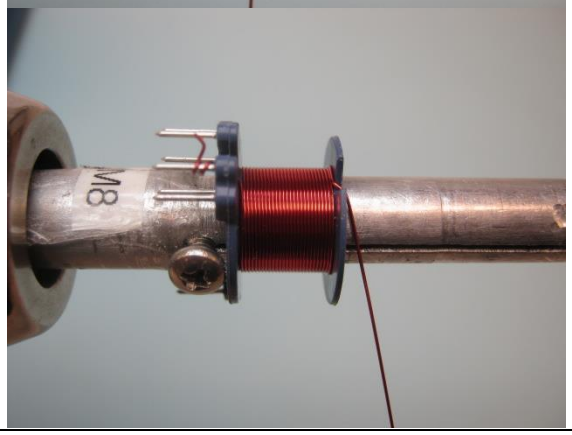
8.1.5 Winding Construction

Winding Preparation	Make a notch on the top secondary side of the bobbin item [2] for secondary wire exit, see illustration above. Position the bobbin item [2] on the mandrel such that the pin side is on the left. Winding direction is clock-wise direction.
WD1 1st Primary	Start at pin 1, wind 27 turns of wire item [4] in 1 layer with tight tension. At the last turn leave the wire ~ 3ft (or 91cm) for WD5 (2nd Primary).
Insulation	Place 1 layer of tape item [8].
WD2 Shield	Use copper shield item [7], start at pin 12 wind 1 full turn with exposed copper side faces inward and leave no-connect at the end.
Insulation	Place 2 layers of tape item [8].
WD3 Secondary	Use wire item [6] leave ~25 mm at start lead A, wind 8 turns in 1 layer. At the last turn, exit the wire at the notch on secondary side and leave ~35 mm floating for end lead B.
Insulation	Place 3 layers of tape item [8].
WD4 Bias	Start at pin 11, wind 4 quad-filar turns of wire item [5], spread evenly in 1 layer, and finish at pin 12.
Insulation	Place1 layer of tape item [8].
WD5 2nd Primary	Use floating wire from WD1-1st Primary, continue winding 26 turns from right to left and finish at pin 2.
Insulation	Place 2 layers of tape item [8].
Finish	Bring the wire floating from WD3- secondary to the left and end with B. Place 2 layers of tape item [8] for insulation and secure all windings. Gap core halves with designated inductance, then assemble and secure clip item [3]. Use wire item [9], solder on 1 side of clip item [3] to connect to pin 12. (see illustration below). Varnish with item [10].

8.1.6 Winding Illustrations

Winding Preparation		Make a notch on the top secondary side of the bobbin item [2] for secondary wire exit, see illustration above. Position the bobbin item [2] on the mandrel such that the pin side is on the left. Winding direction is clock-wise direction.
WD1 **1st Primary**	 	Start at pin 1, wind 27 turns of wire item [4] in 1 layer with tight tension. At the last turn leave the wire ~3 ft (or 91 cm) for WD5 (2nd Primary).

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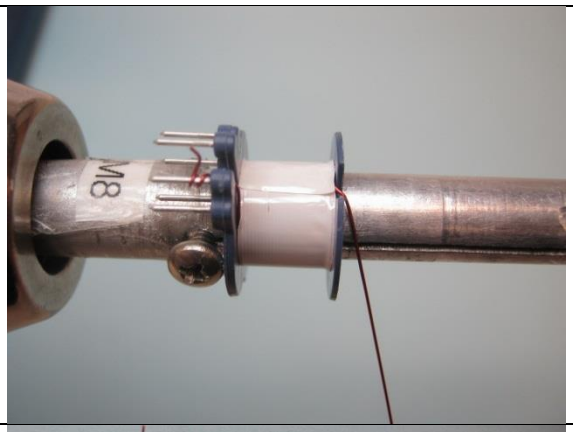
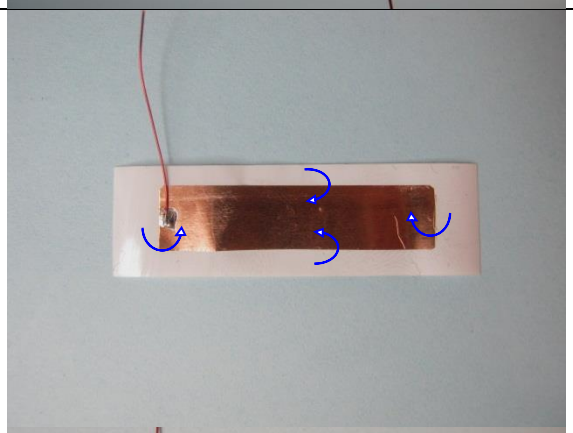
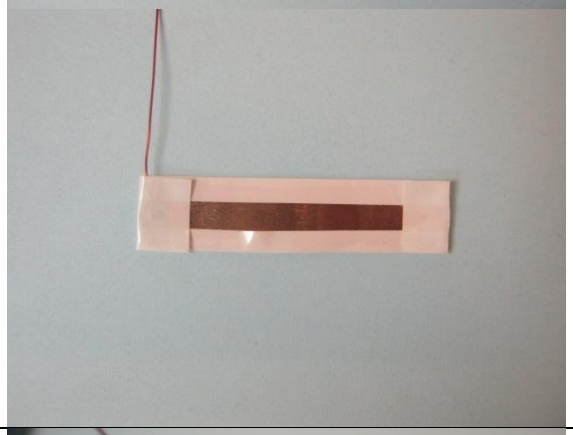
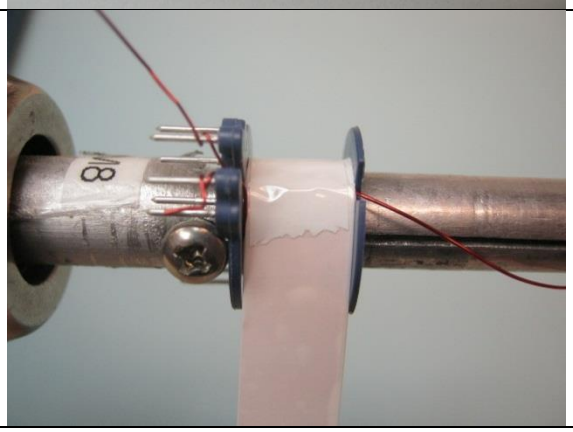
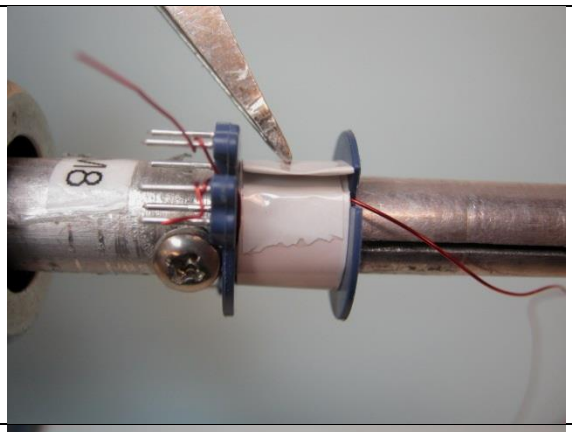
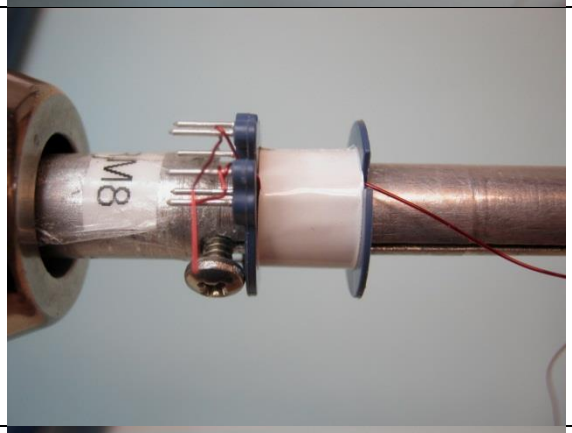
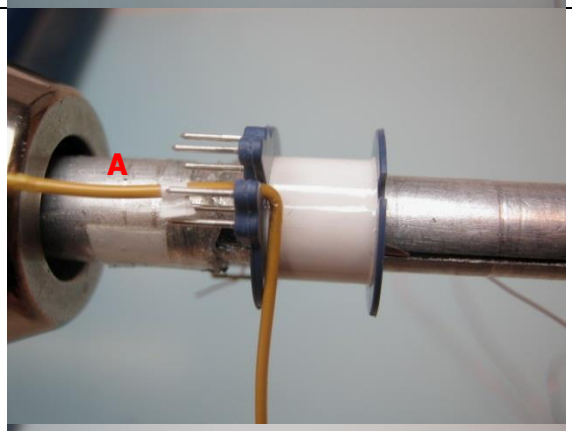
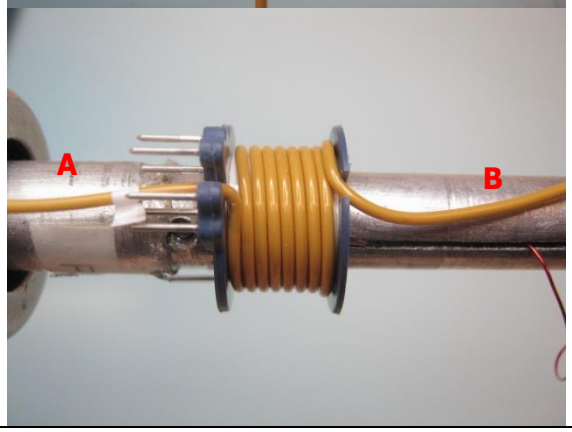
Insulation		Place 1 layer of tape item [8].
Copper foil construction	 	Wrap tape (15.0 mm wide) around the copper foil.
WD2 Shield		Use copper shield item [7], start at pin 12 wind 1 full turn with exposed copper side faces inward and leave no-connect at the end.

		
Insulation		Place 2 layers of tape item [8].
WD3 Secondary	 	Use wire item [6] leave ~25 mm at start lead A, wind 8 turns in 1 layer. At the last turn, exit the wire at the notch on secondary side and leave ~35 mm floating for end lead B.

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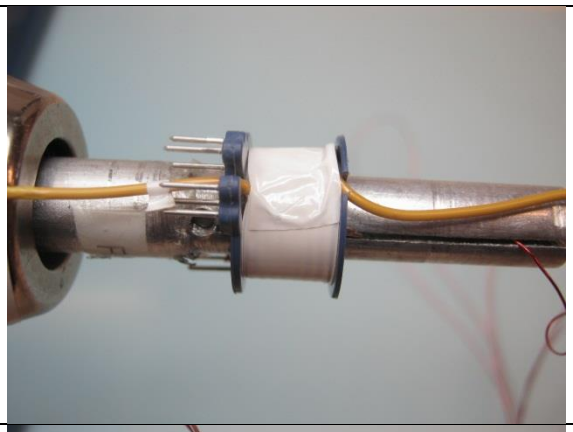
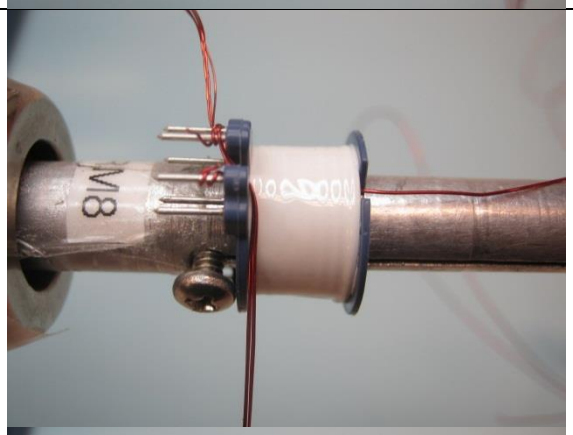
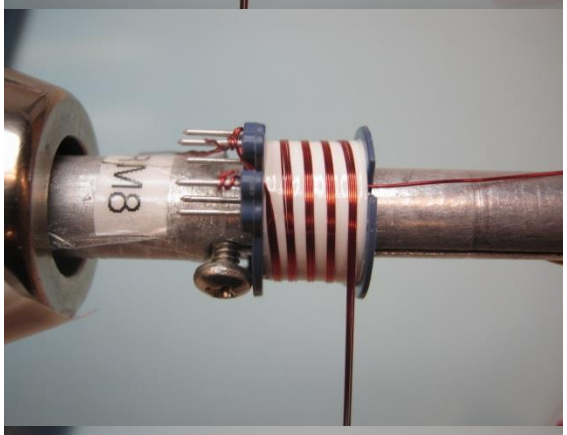
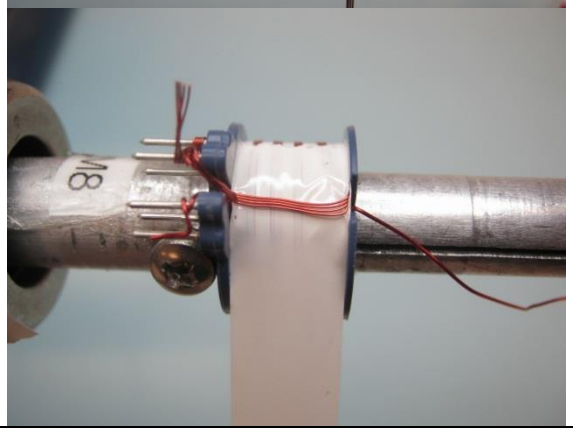
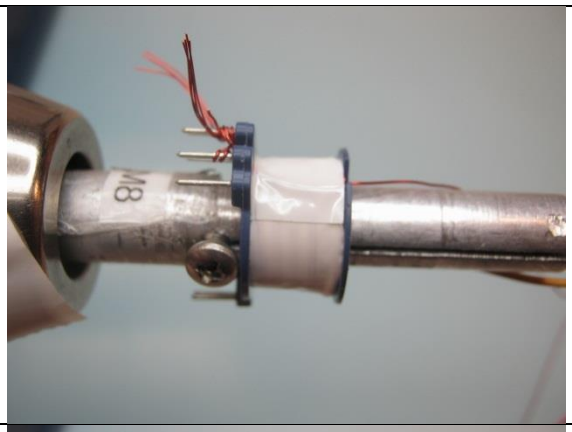
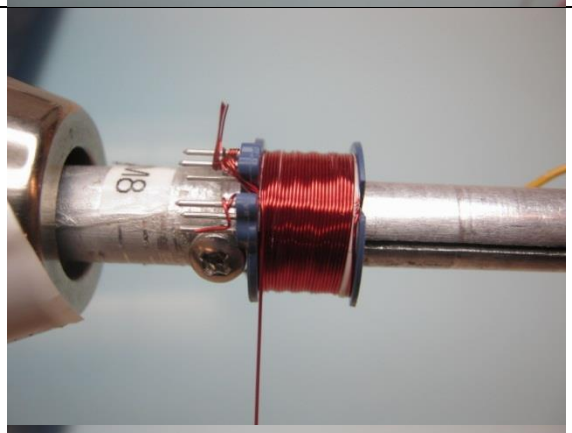
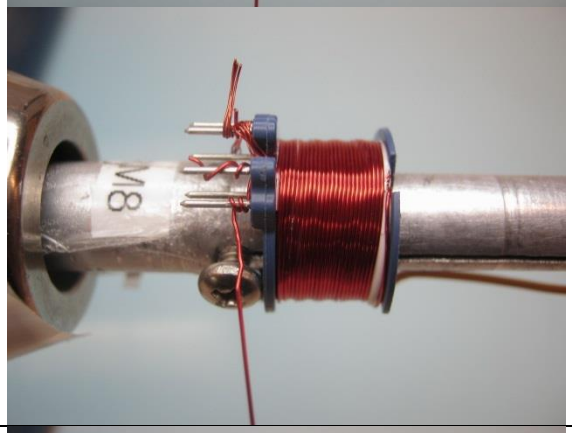
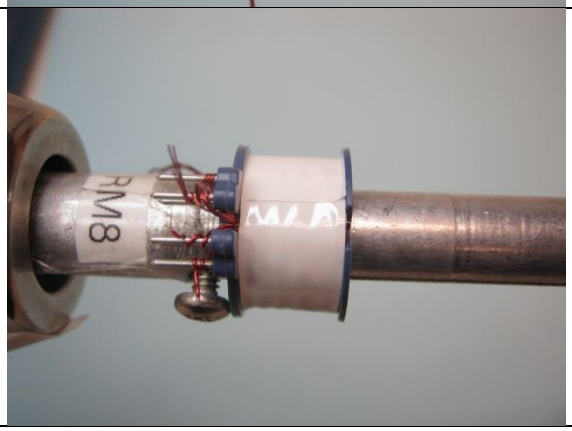
Insulation		Place 3 layers of tape item [8].
WD4 **Bias**	  	Start at pin 11, wind 4 quad-filar turns of wire item [5], spread evenly in 1 layer, and finish at pin 12.

Insulation		Place 1 layer of tape item [8].
WD5 **2nd Primary**	 	Use floating wire from WD1-1st Primary, continue winding 26 turns from right to left and finish at pin 2.
Insulation		Place 2 layers of tape item [8].

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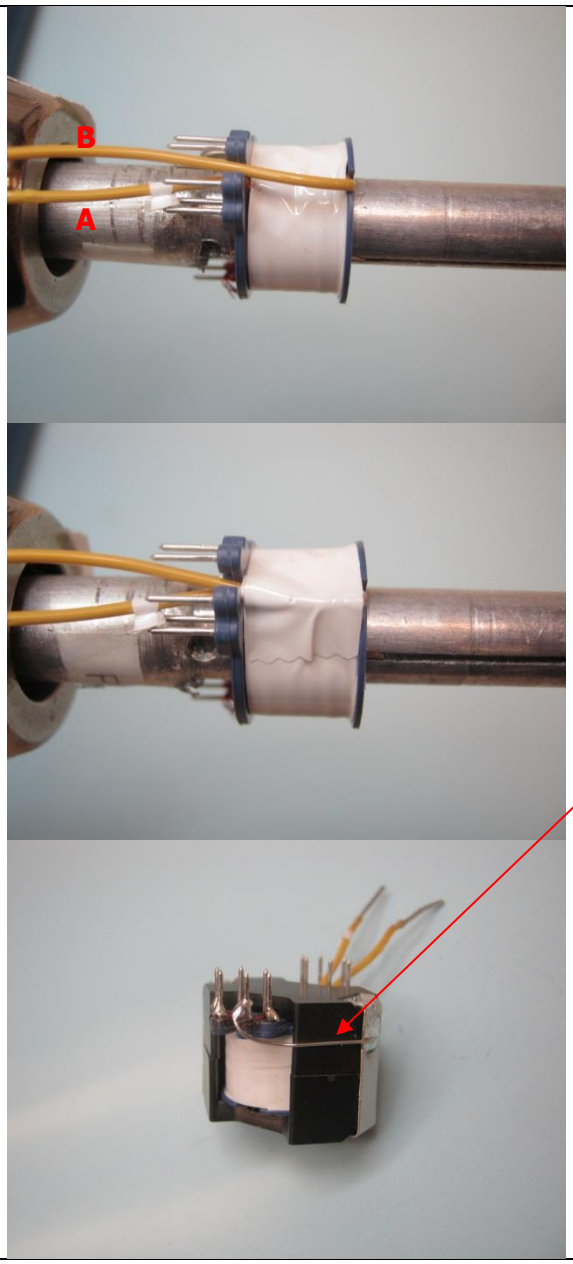
Finish		Bring the wire floating from WD3- secondary to the left and end with B. Place 2 layers of tape item [8] for insulation and secure all windings. Gap core halves with designated inductance, then assemble and secure clip item [3]. Use wire item [9], solder on 1 side of clip item [3] to connect to pin 12. Varnish with item [10].

8.2 *Inductor L1 Specification*

8.2.1 Electrical Diagram

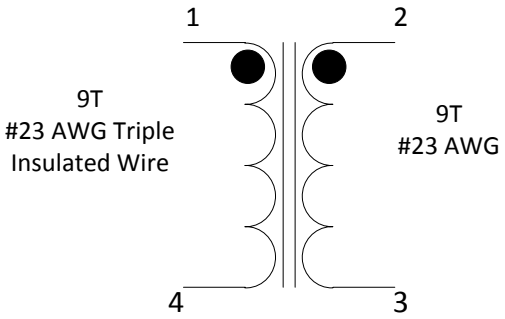


Figure 10 – Inductor Electrical Diagram.

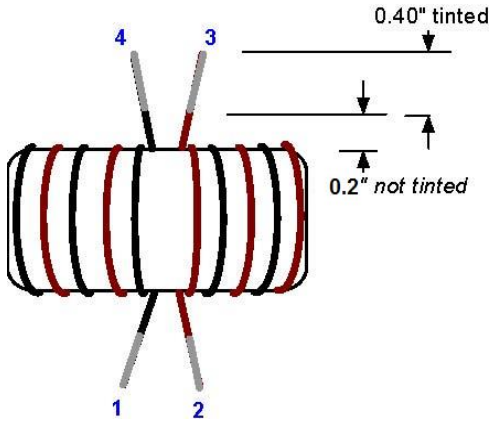
8.2.2 Electrical Specifications

Inductance	Pins 1-4 measured at 100 kHz, 0.4 V_{RMS}.	200 µH ±10%
Resonant Frequency	Pins 1-4, all other windings open.	>300 KHz
Primary Leakage Inductance	Pins 1-4, with 2-3 shorted.	1 µH

8.2.3 Material List

Item	Description
[1]	Core: GL50 T 12X6X4-C, BIPOLAR ELECTRONIC CO., LTD
[2]	Magnet Wire: #23 AWG.
[3]	Triple Insulated wire #23 AWG.

8.2.4 Illustration



Note: Add Teflon sleeving for terminations.

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8.3 *Inductor L2 Specification*

8.3.1 Electrical Diagram

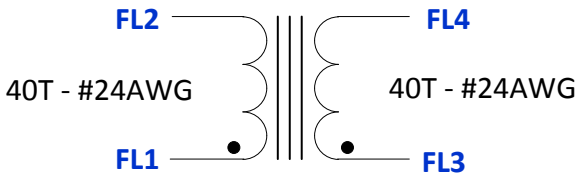


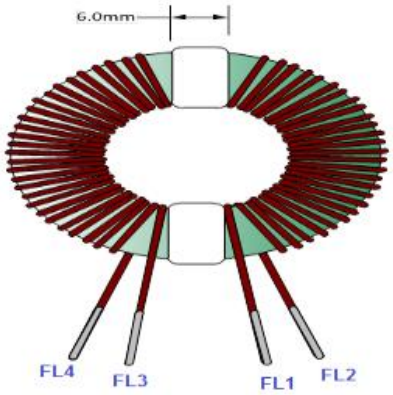
Figure 11 –Inductor Electrical Diagram.

8.3.2 Electrical Specifications

Inductance	Pins FL1-FL2 measured at 100 kHz, 0.4 V_{RMS}.	13 mH ±15%
Primary Leakage Inductance	Pins FL1-FL2, with FL3-FL4 shorted.	62 µH

8.3.3 Material List

Item	Description
[1]	Core: JL15 (JLW ELECTRONICS (HONG KONG) LIMITED). AL = 8000 nH/N^2. Mfg P/N: T18x10x7C-JL15*. PI P/N: 30-00398-00.
[2]	Magnetic Wire: #24 AWG, double coated.
[3]	Margin tape: 3M44, cream, 6.0 mm wide.
[4]	Divider -- Fish paper, insulating cotton rag, 0.032” thick, PI #: 66-00042-00. Cut to size 10.0 mm x 9.0 mm.



8.3.4 Winding Instructions

1. Place margin tape item [3] on the core item [1] to divide into 2 sections equally. Two windings will be wound in each section separately.
2. Mark on 1 side of margin tape as start side, use ~ 3 ½ ft. of wire item [2], start at middle of the wire, designate start lead as FL1, wind 13 turns from start side from left to right and leave floating as FL2.
3. Take FL1 wire, wind 11 turns on 2nd layer also from left to right.
4. Now take FL2 wire, wind 8 turns on 3rd layer from right to left.
5. Take FL1 wire, wind 8 turns on 4th layer from right to left. Note that now both leads FL1 and FL2 go back to start side.
6. Continue winding for another section same as this section winding, same direction, also start from start side as marked, with start lead as FL3 and other as FL4.
7. Insert 4 pieces of item [4] in the center to make more isolation between windings.
8. Tin all leads.

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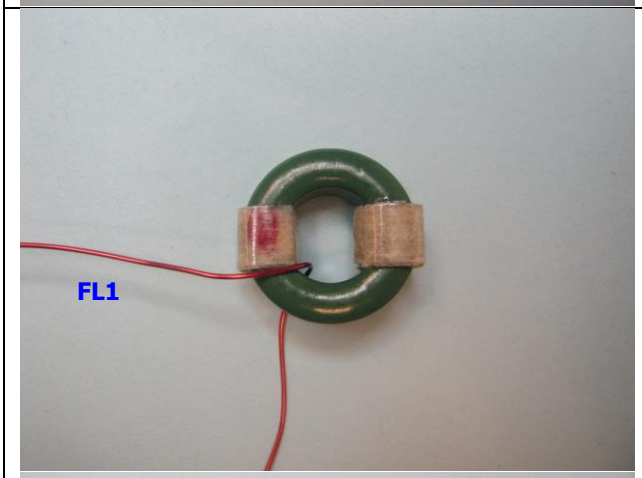
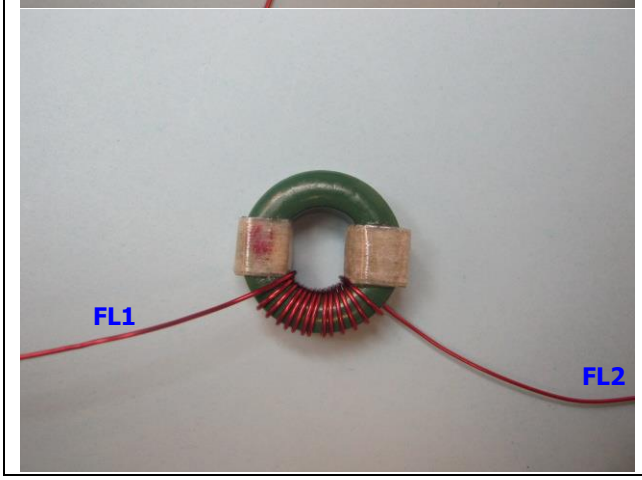
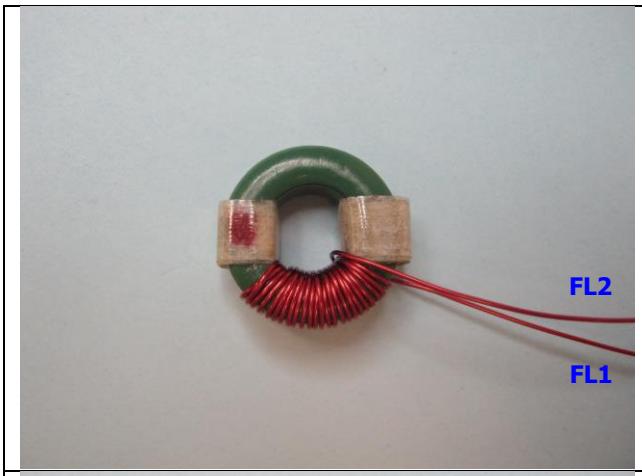
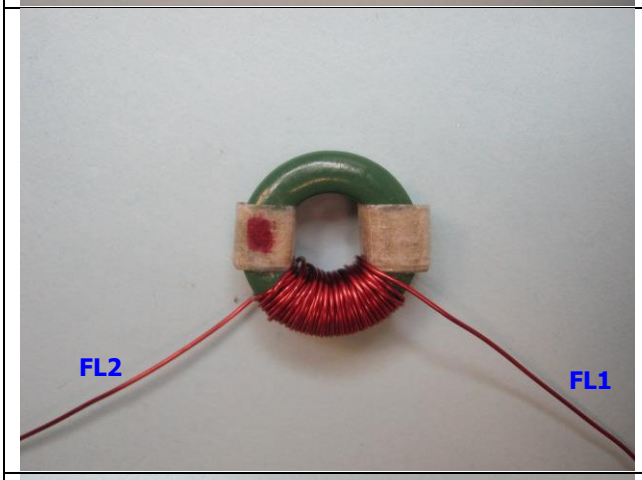
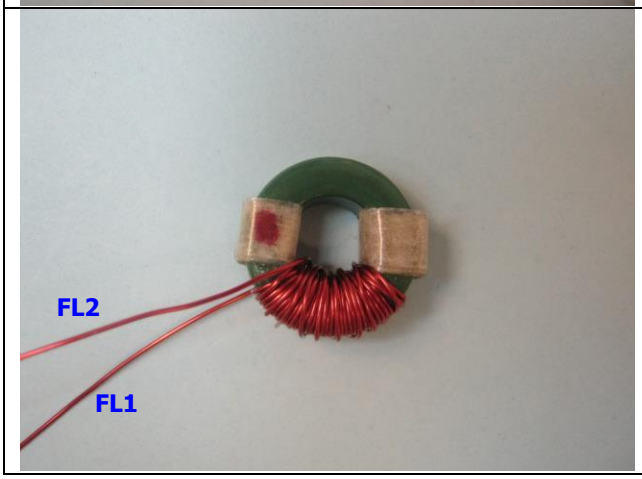
8.3.5 Winding Illustrations

	Place margin tape item [3] on the core item [1] to divide into 2 sections equally. Two windings will be wound in each section separately.
 	Mark on 1 side of margin tape as start side, use ~ 3 ½ ft. of wire item [2], start at middle of the wire, designate start lead as FL1, wind 13 turns from start side from left to right and leave floating as FL2.

	Take FL1 wire, wind 11 turns on 2nd layer also from left to right.
	Now take FL2 wire, wind 8 turns on 3rd layer from right to left.
	Take FL1 wire, wind 8 turns on 4th layer from right to left. Note that now both leads FL1 and FL2 go back to start side.

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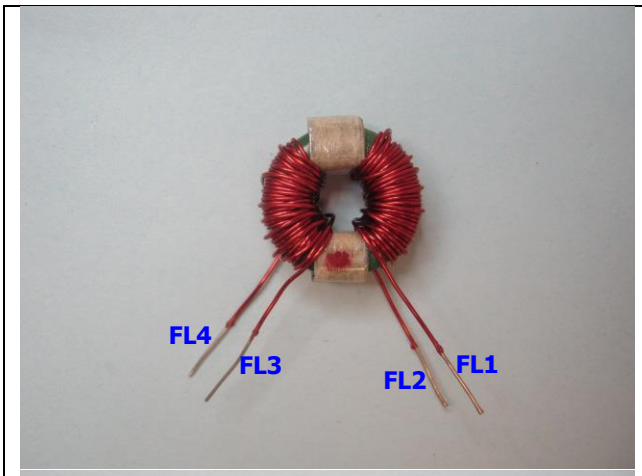
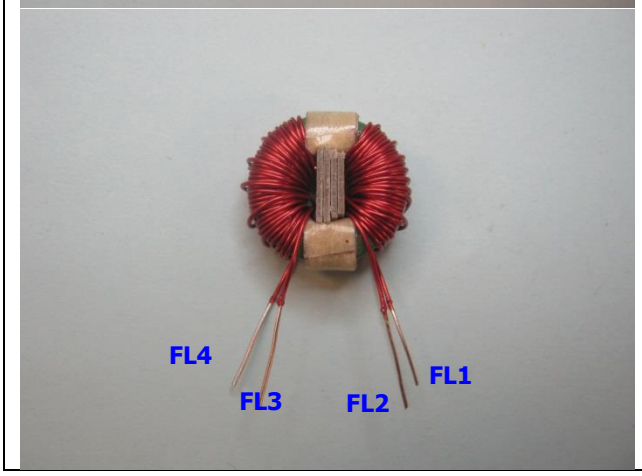


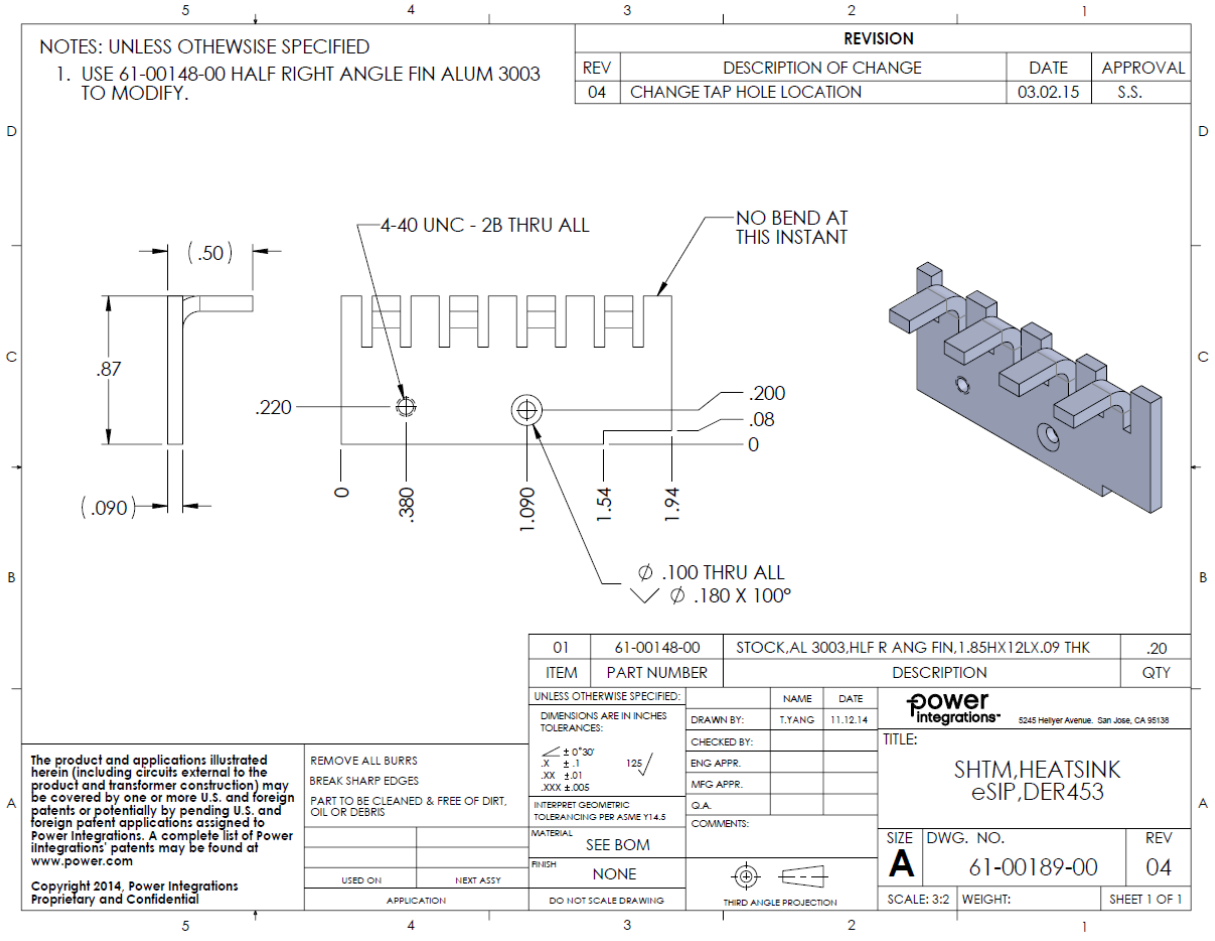


Continue winding for another section same as this section winding, same direction, also start from start side as marked, with start lead as FL3 and other as FL4.
Insert 4 pieces of item [4] in the center to make more isolation between windings.
Tin all leads.

9 Heat Sink Assemblies

9.1 *eSIP Heat Sink*

9.1.1 eSIP Heat Sink Fabrication Drawing



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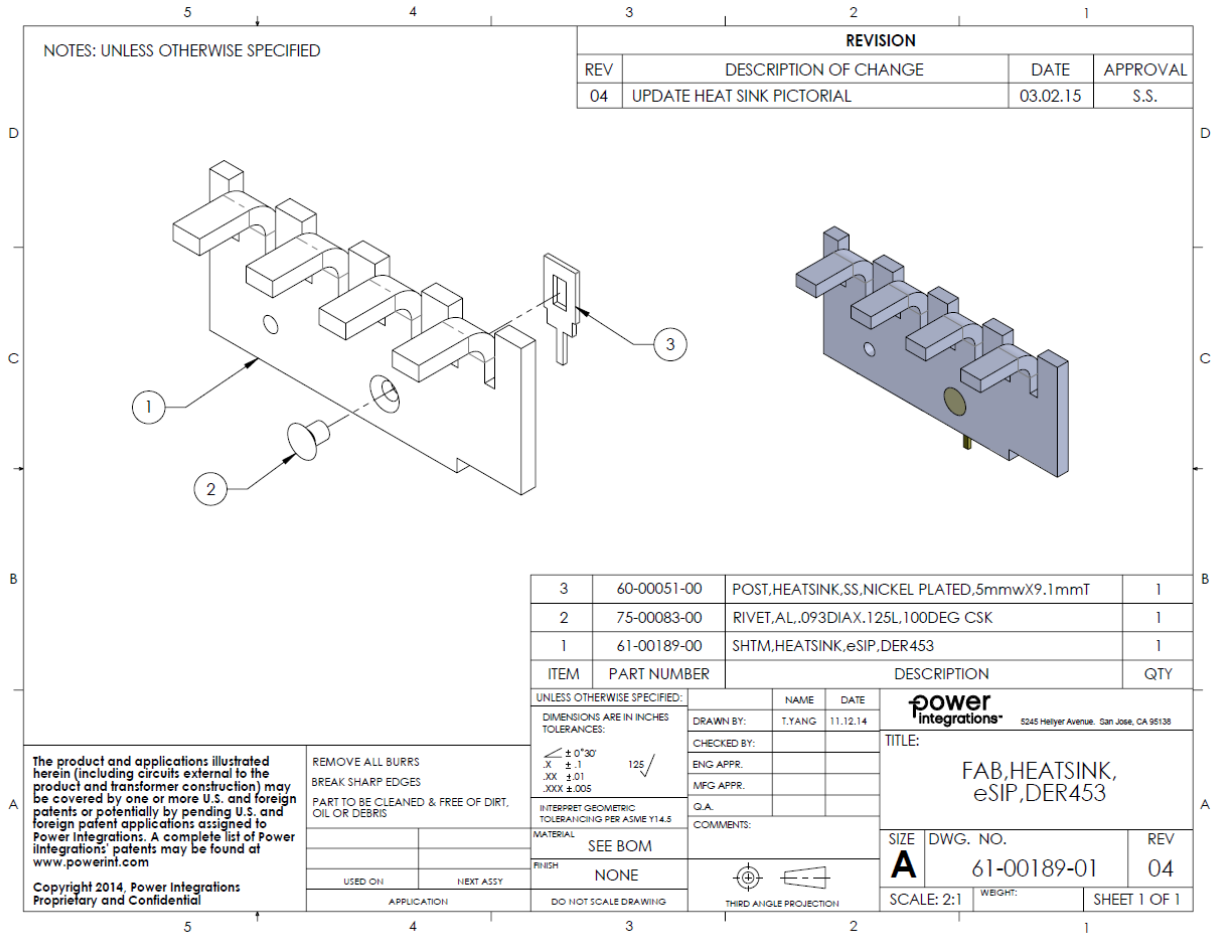
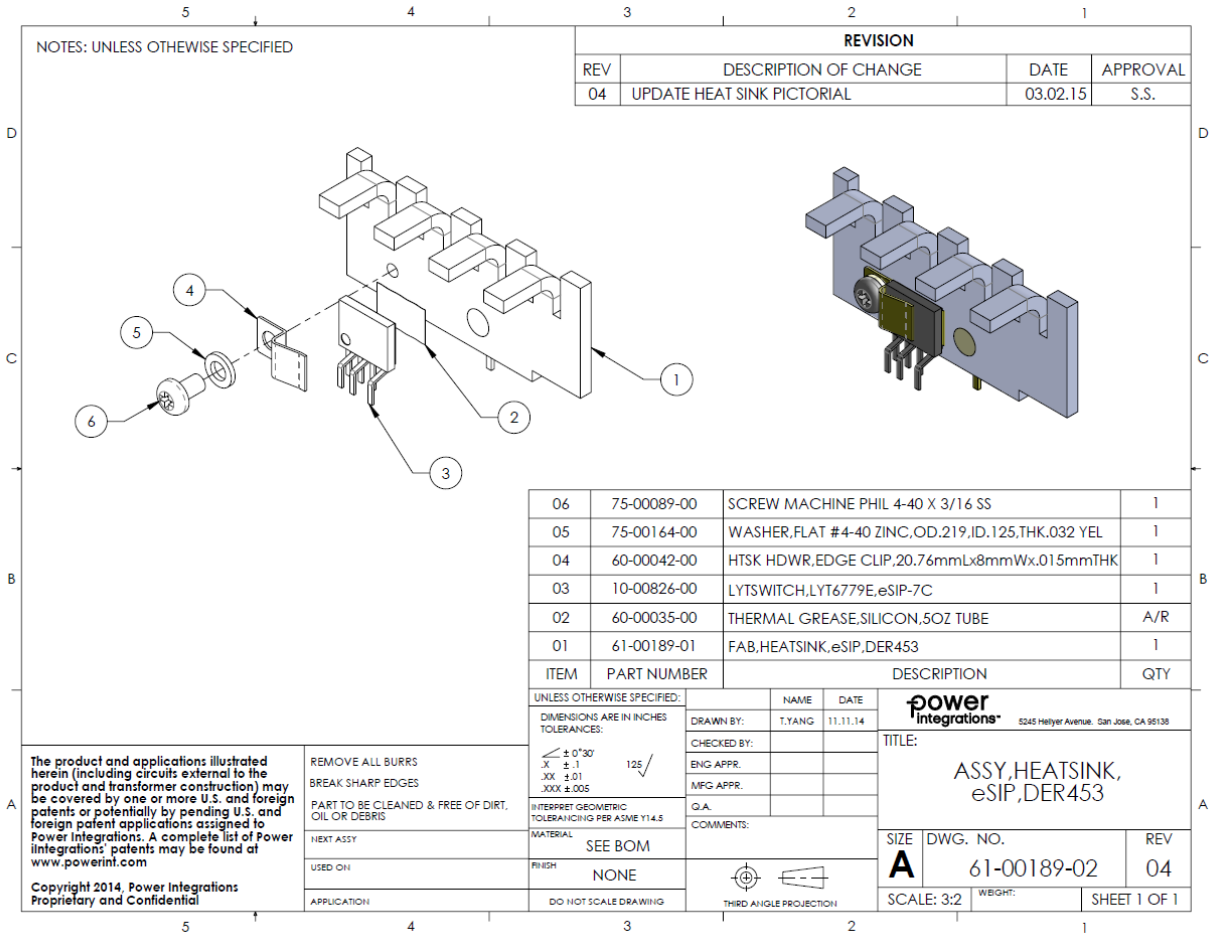
9.1.2 eSIP Heat Sink Assembly Drawing



9.1.3 eSIP and Heat Sink Assembly Drawing



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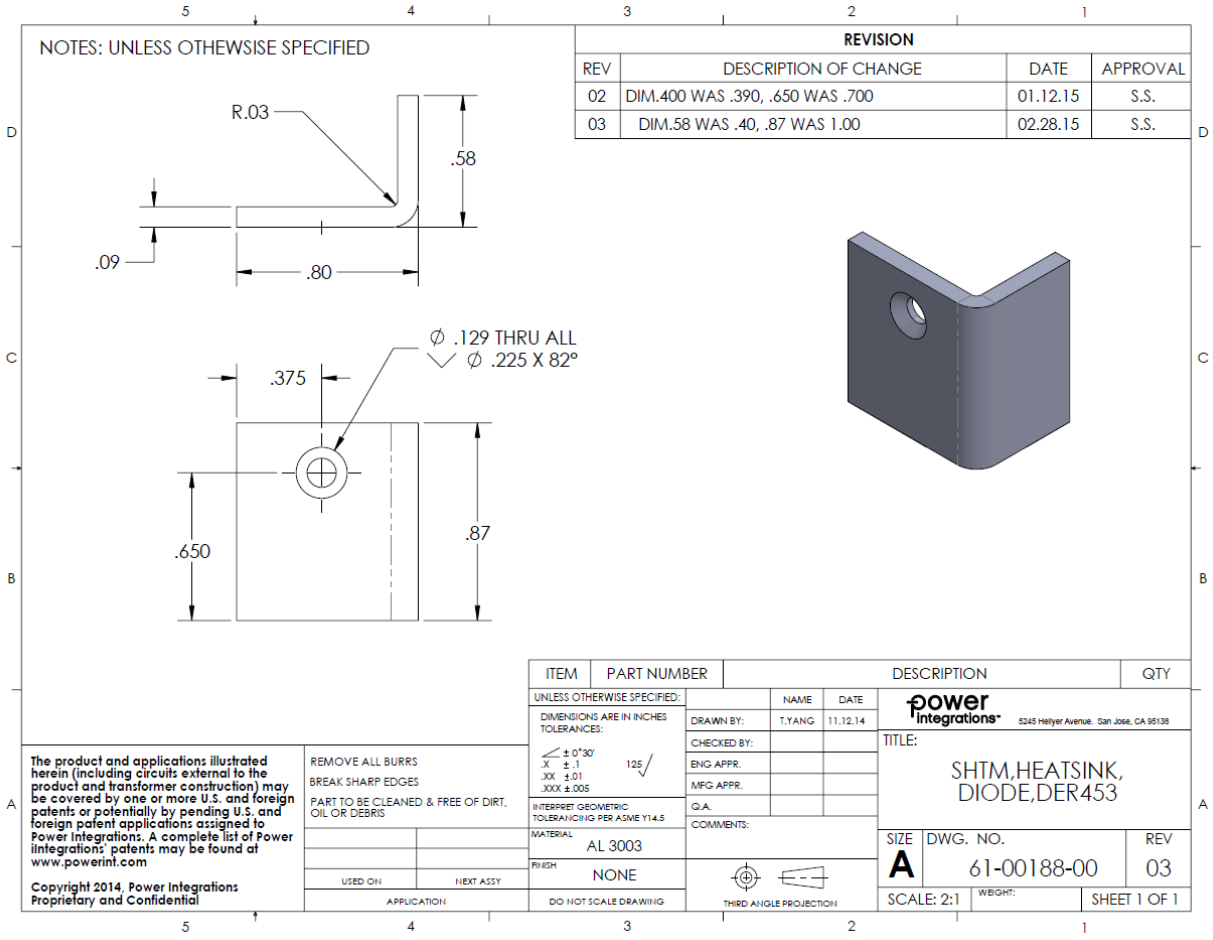
9.2 ***Diode Heat Sink***

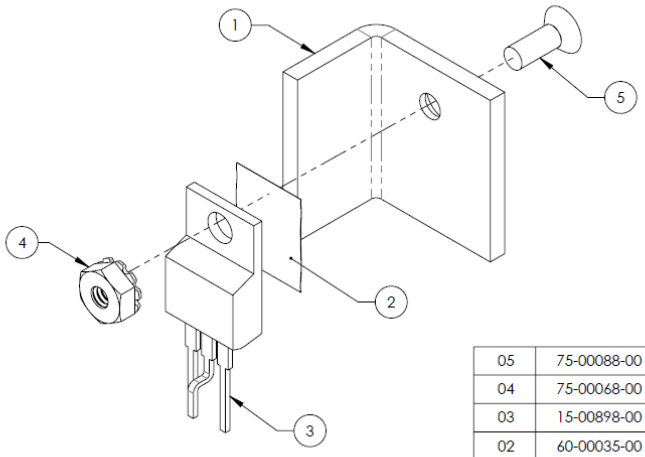
9.2.1 Diode Heat Sink Fabrication Drawing

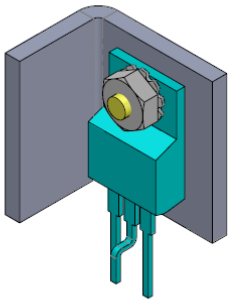


9.2.2 Diode and Heat Sink Assembly Drawing

NOTES: UNLESS OTHERWISE SPECIFIED

REVISION			
REV	DESCRIPTION OF CHANGE	DATE	APPROVAL
02	UPDATE HSK PICTORIAL, CHG ITEM 3 P/N	01.12.15	S.S.
03	UPDATE HSK PICTORIAL	02.28.15	S.S.





ITEM	PART NUMBER	DESCRIPTION	QTY
05	75-00088-00	SCREW,MACHINE PHIL FLAT HEAD 4-40 X 5/16 SS	1
04	75-00068-00	NUT,HEX,KEP 4-40,S ZN Cr3 PLATE RoHS	1
03	15-00898-00	100V,10A,DUAL SCHOTTKY,TO220FP	1
02	60-00035-00	THERMAL GREASE,SILICONE,5OZ TUBE	A/R
01	61-00188-00	SHTM,HEATSINK,DIODE,DER453	1

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
∠ ± 0°30'
.X ±.1
.XX ±.01
.XXX ±.005
125
INTERPRET GEOMETRIC TOLERANCING PER ASME Y14.5
MATERIAL: SEE BOM
FINISH: NONE
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	T.YANG	11.18.14
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

THIRD ANGLE PROJECTION

power integrations 5245 Hellyer Avenue. San Jose, CA 95138

TITLE: ASSY,HEATSINK, DIODE,DER453

SIZE	DWG. NO.	REV
A	61-00188-02	03
SCALE: 2:1	WEIGHT:	SHEET 1 OF 1

REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS

USED ON | NEXT ASSY
APPLICATION

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10 Performance Data

All measurements performed at room temperature and 50/60 Hz line frequency, except where otherwise stated. For all tests, the full load was 2.37 A.

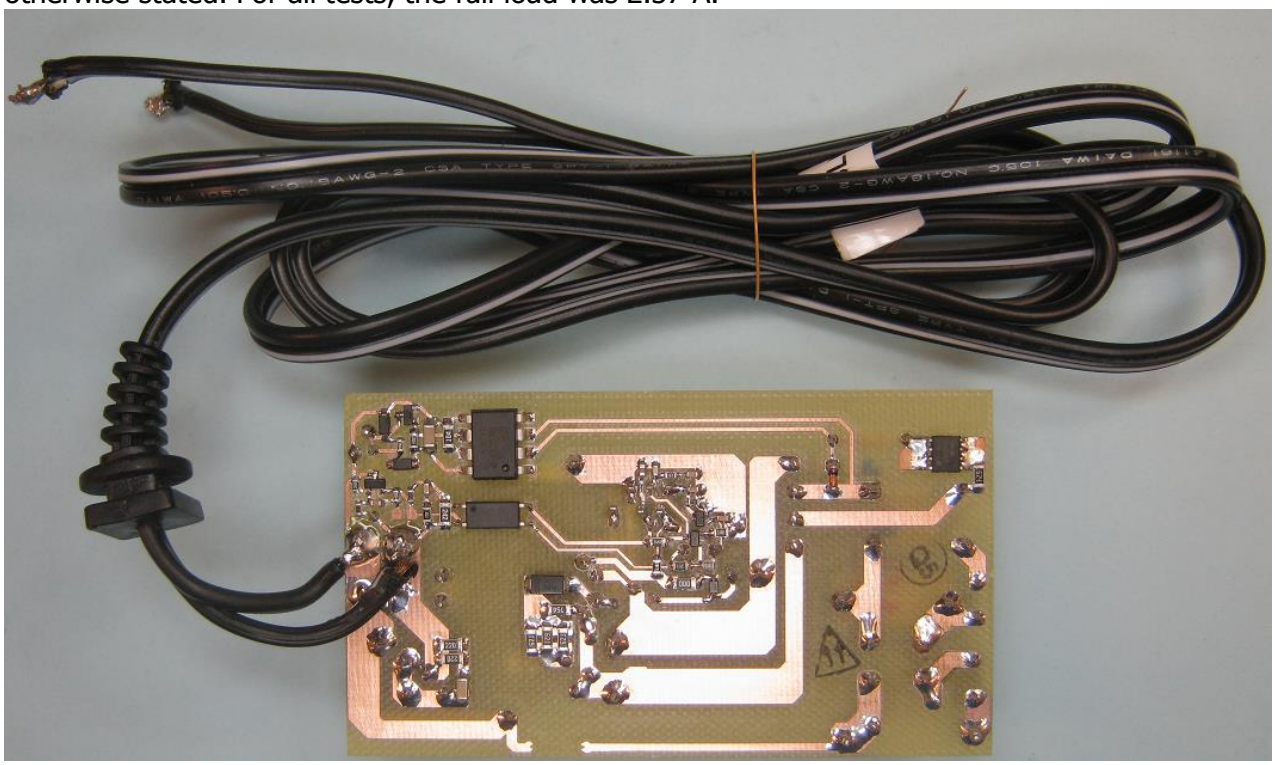

Figure 12 – Output Cable, #18 AWG, 1.8 M.

Note: All the performance measurements were done at the end of the cable.

10.1 *Active Mode Efficiency*

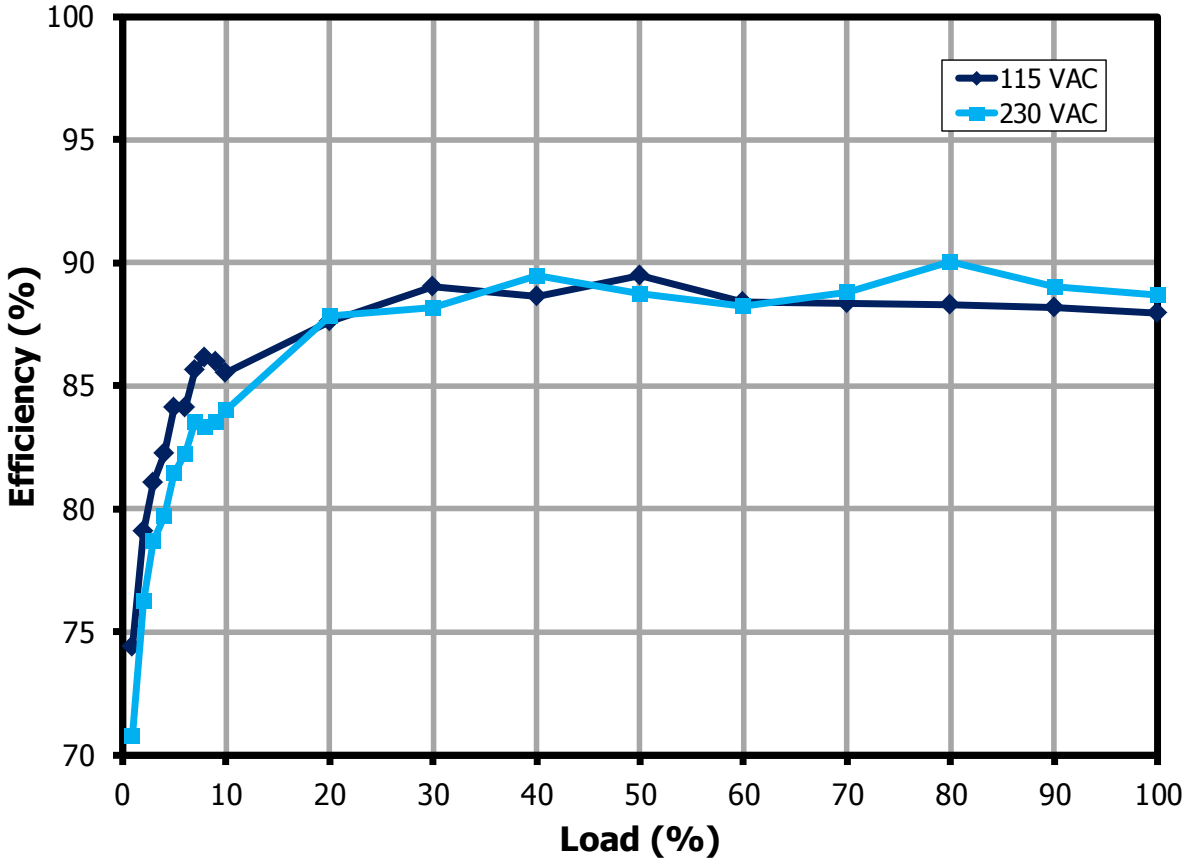

Figure 13 – Active Mode Efficiency, Room Temperature.

115 VAC				230 VAC			
V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	η (%)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	η (%)
19.247	0.5891	12.91	87.8	19.247	0.5888	12.82	88.4
19.195	1.1801	25.34	89.4	19.193	1.1807	25.52	88.8
19.144	1.771	38.43	88.2	19.142	1.772	37.78	89.8
19.091	2.371	51.47	87.9	19.09	2.371	51.01	88.7
		Avg.	**88.3**			**Avg.**	**88.9**

Table 1 – Four Point Average Efficiency (25%, 50%, 75% and 100%), Room Temperature.

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10.2 *Full Load Efficiency*

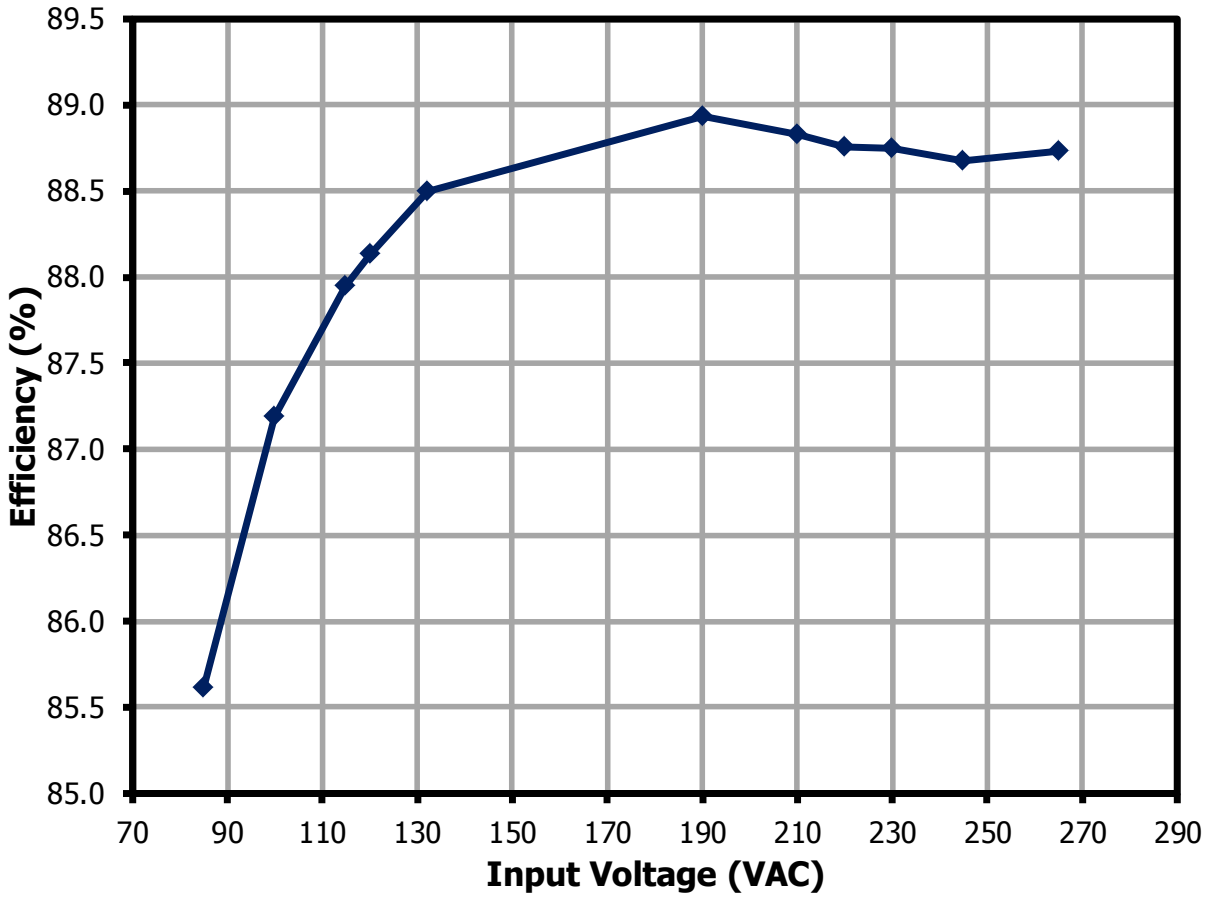

Figure 14 – Full Load Efficiency vs. Input Voltage, Room Temperature.

10.3 *No-Load Input Power*

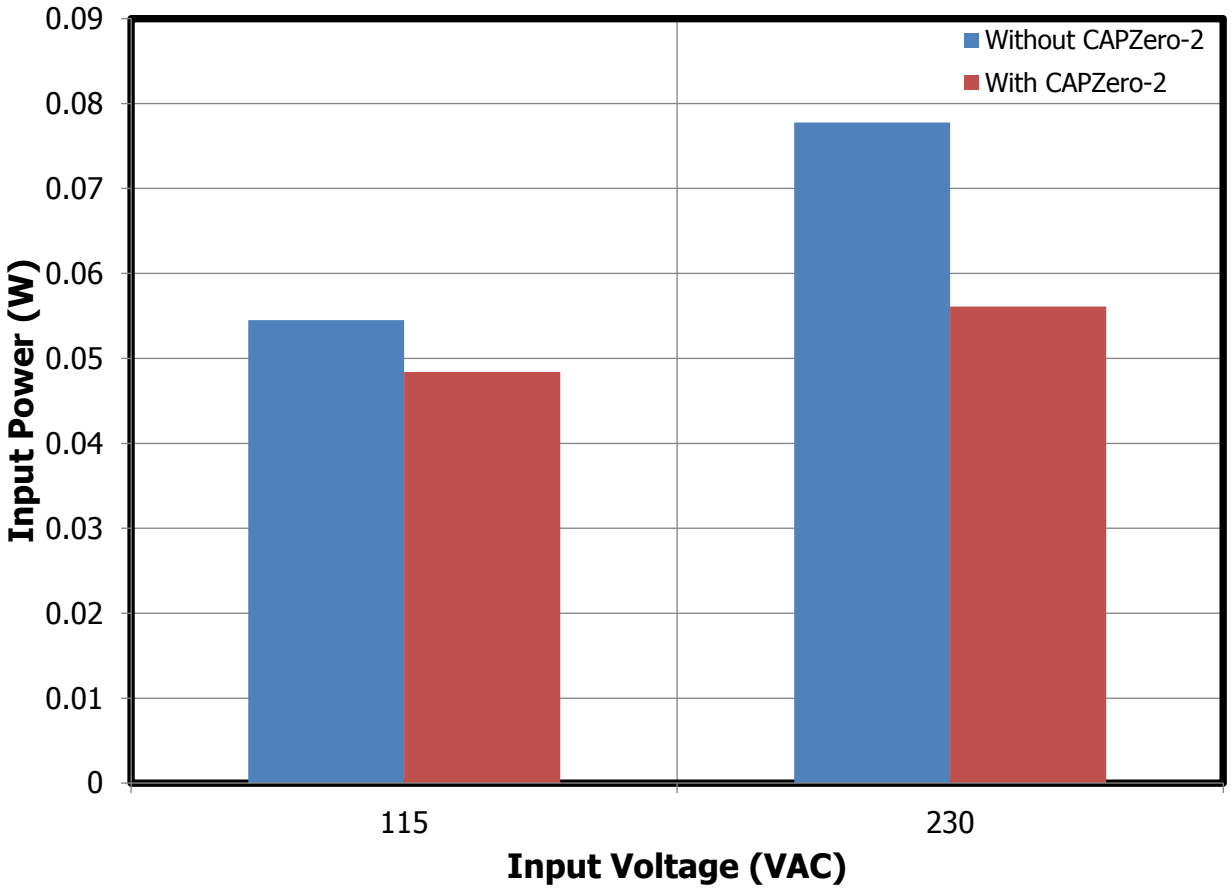

Figure 15 – No-Load Input Power vs. Input Voltage, Room Temperature.

Note: 1.86 MΩ resistor was used as an x-capacitor discharge resistor when CAPZero-2 was not used.

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10.4 *Light Load Input Power*

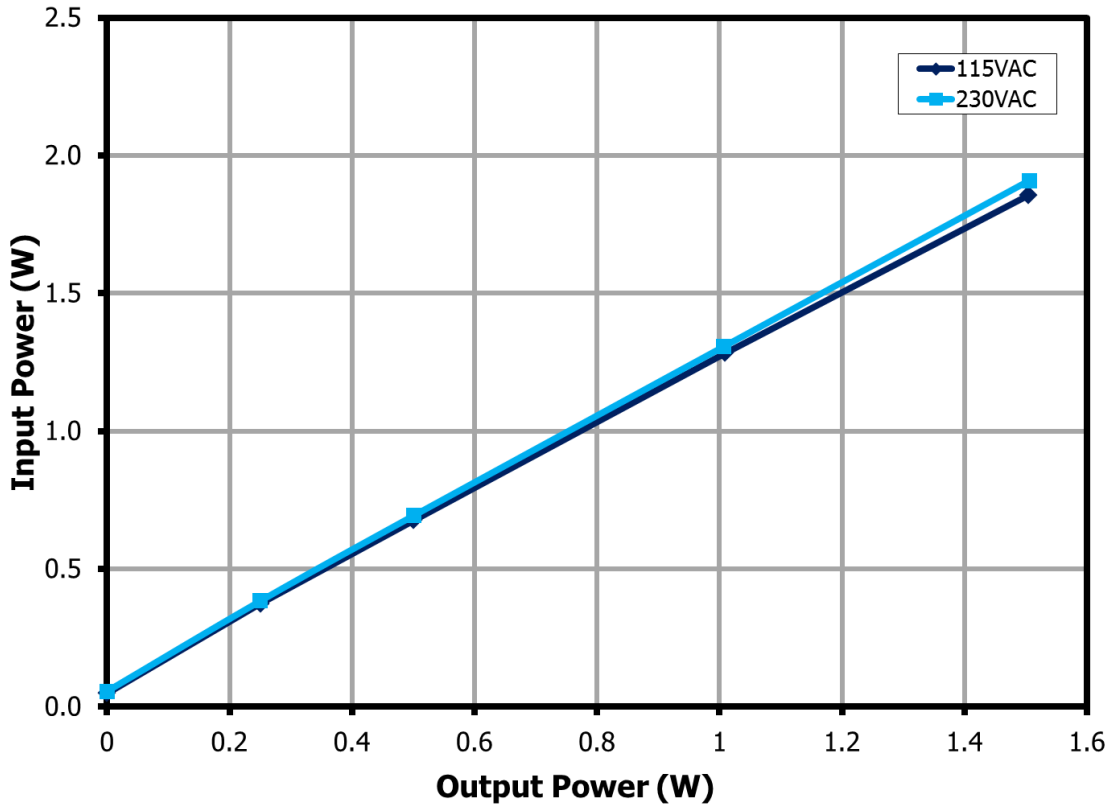

Figure 16 – Input Power vs. Output Power, Room Temperature.

10.5 *Line Regulation*

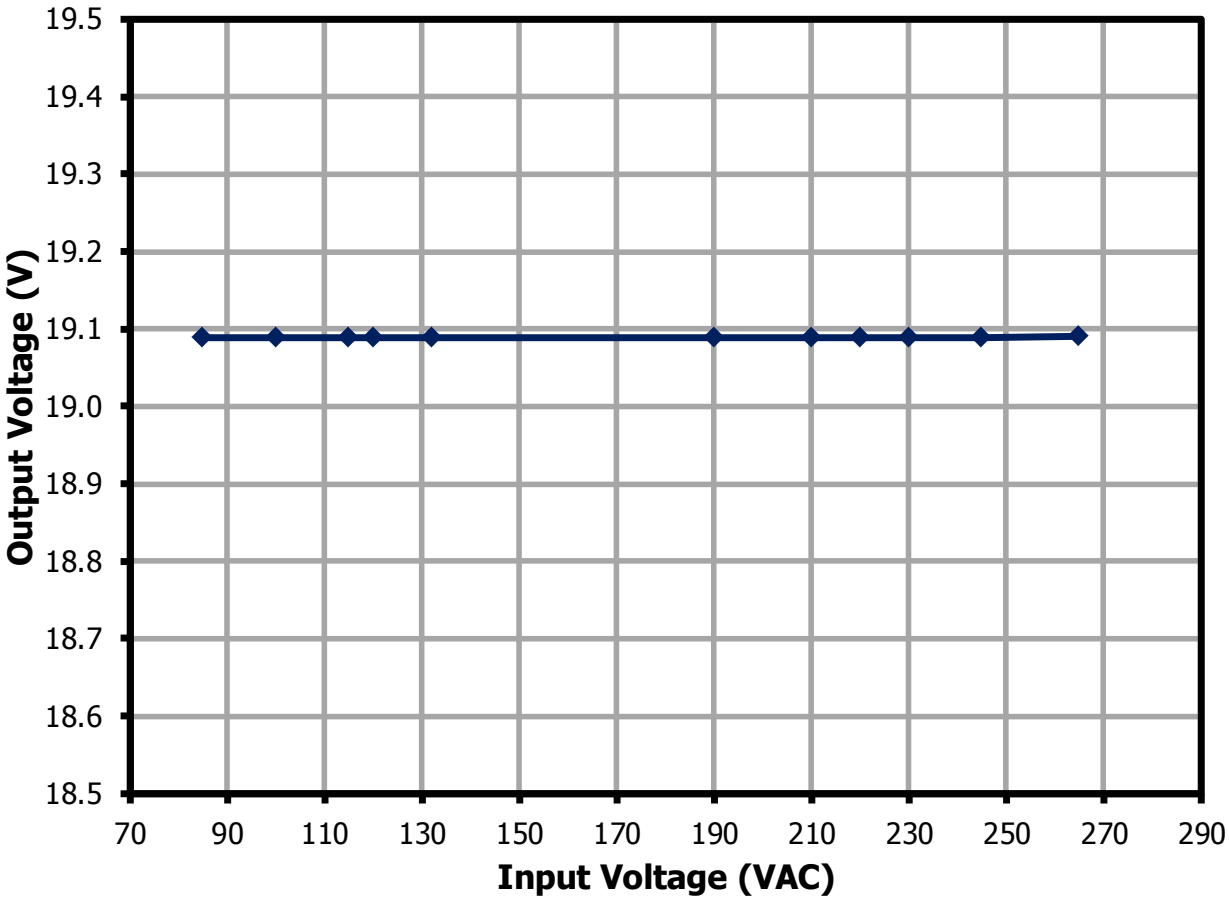

Figure 17 – Line Regulation under Full Load, Room Temperature.

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10.6 *Load Regulation*

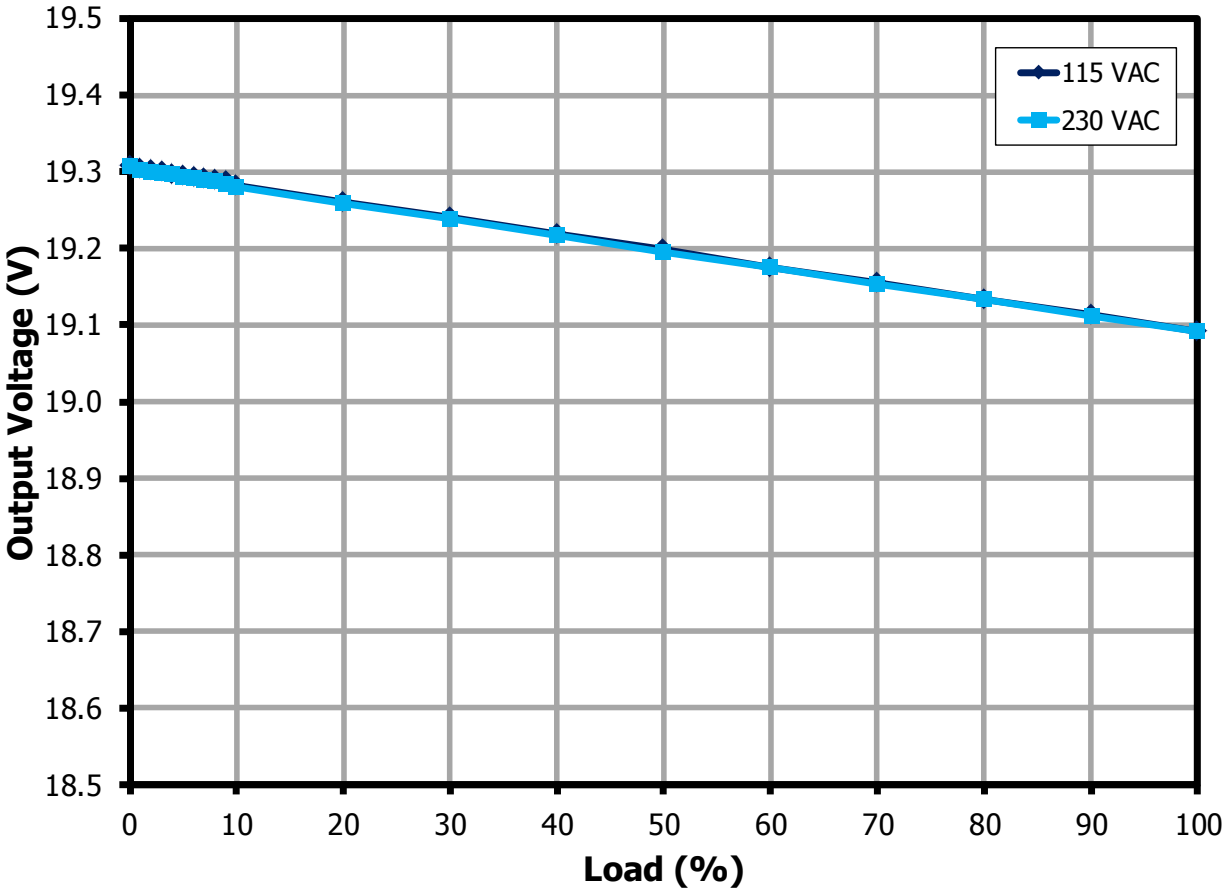

Figure 18 – Load Regulation, Room Temperature.

11 Waveforms

11.1 *Zero Crossing Detection*

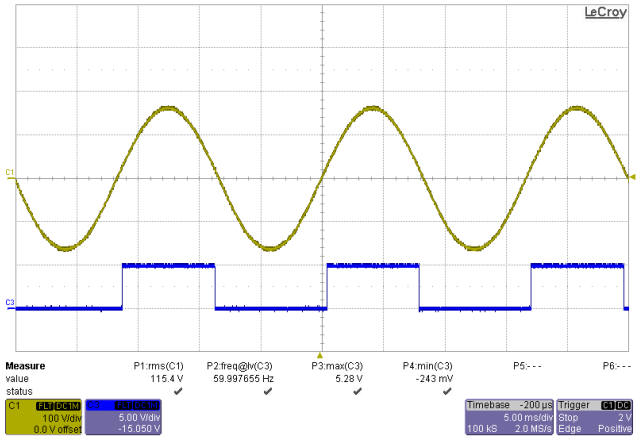

Figure 19 – 115 VAC, No-Load.
Upper: V_{IN}, 100 V / div.
Lower: V_{ZCD}, 5 V / div., 5 ms / div.

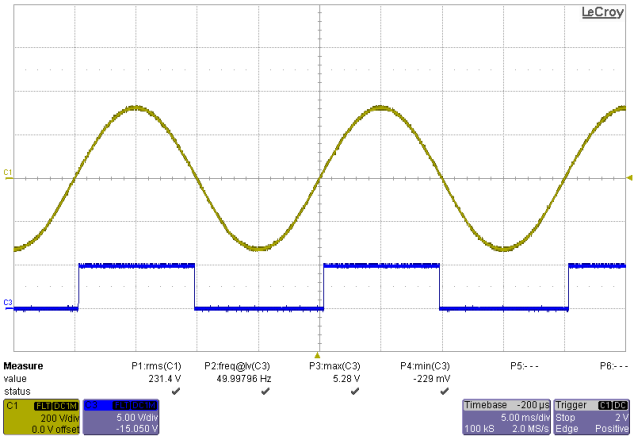

Figure 20 – 230 VAC, No-Load.
Upper: V_{IN}, 200 V / div.
Lower: V_{ZCD}, 5 V / div., 5 ms / div.

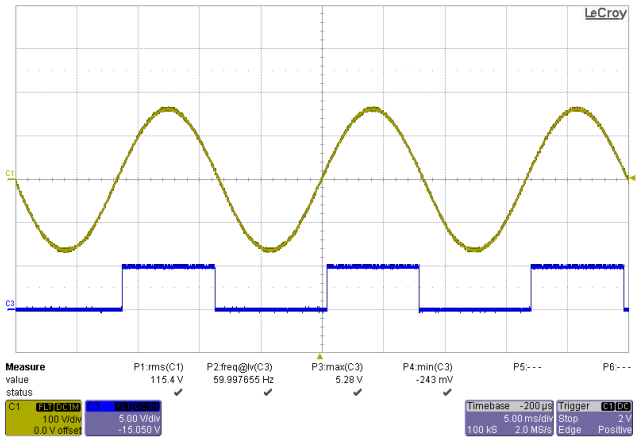

Figure 21 – 115 VAC, Full Load.
Upper: V_{IN}, 100 V / div.
Lower: V_{ZCD}, 5 V / div., 5 ms / div.

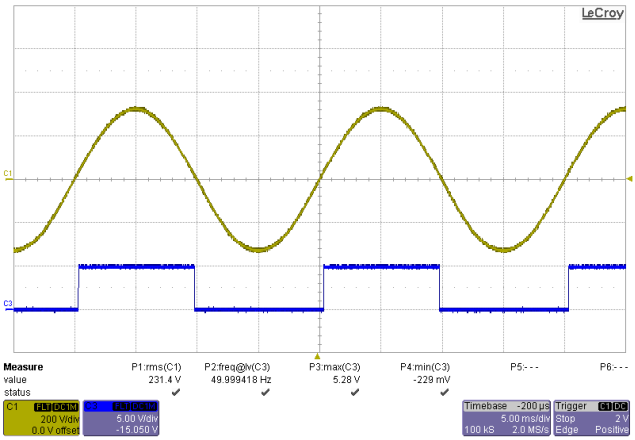

Figure 22 – 230 VAC, Full Load.
Upper: V_{IN}, 200 V / div.
Lower: V_{ZCD}, 5 V / div., 5 ms / div.

Note: Where V_{ZCD} is input AC zero crossing detection signal.

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11.2 *Drain Voltage and Current, Normal Operation*

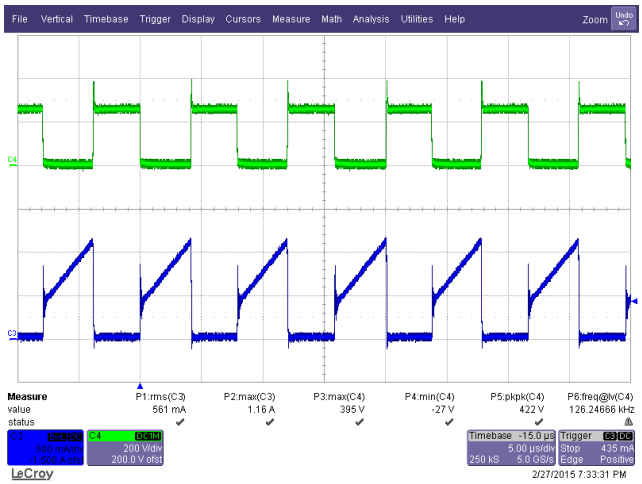

Figure 23 – 90 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A / div., 5 μs / div.

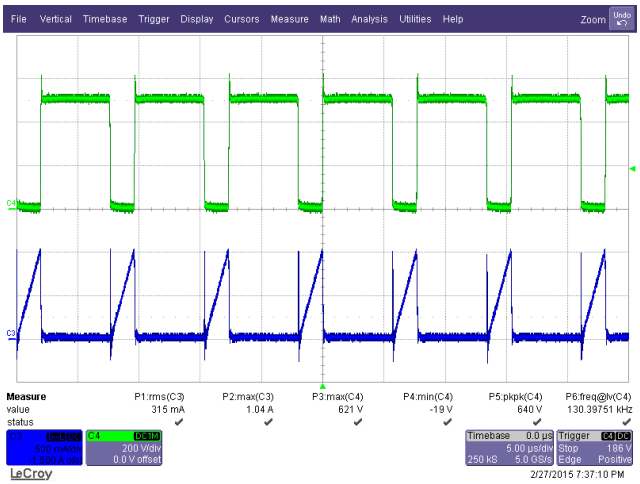

Figure 24 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A / div., 5 μs / div.

11.3 *Drain Voltage and Current Start-Up Profile*

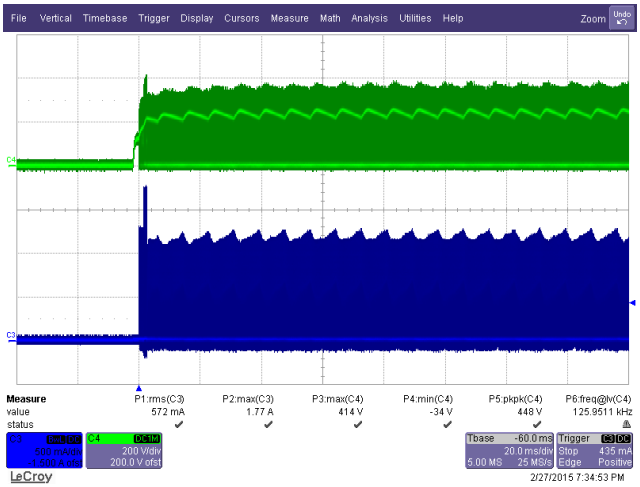

Figure 25 – 90 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A, 2 ms / div.

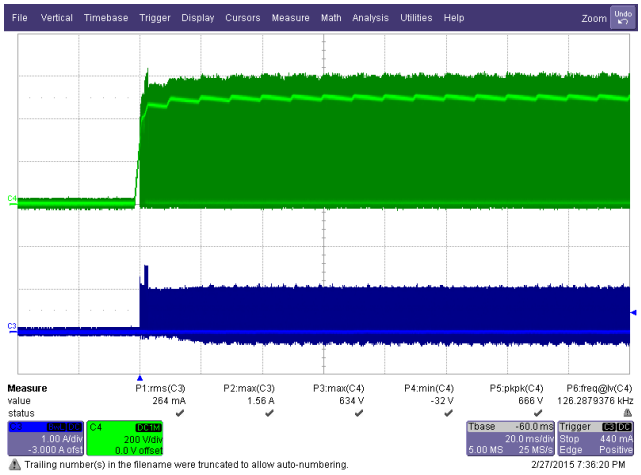

Figure 26 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A, 2 ms / div.

11.4 *Load Transient Response*

In the figures shown below, the output was AC coupled to view the load transient response. The oscilloscope was triggered using the load current step as a trigger source.

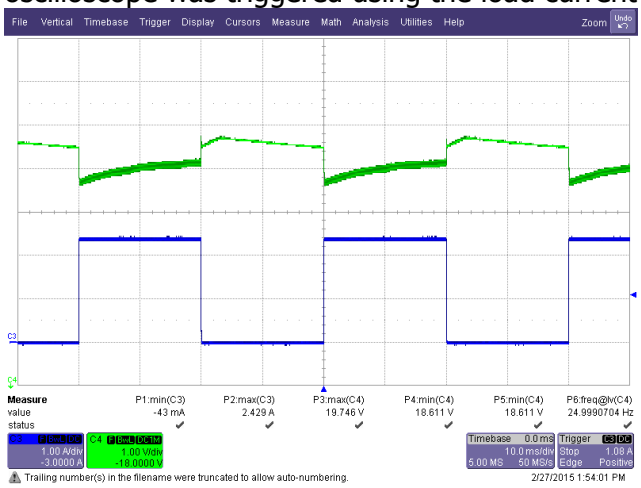

Figure 27 – Transient Response, 90 VAC, 0%<-->100% Step Load. Upper: V_{OUT}, 1 V / div. Lower: I_{OUT}, 1 A / div., 10 ms / div.

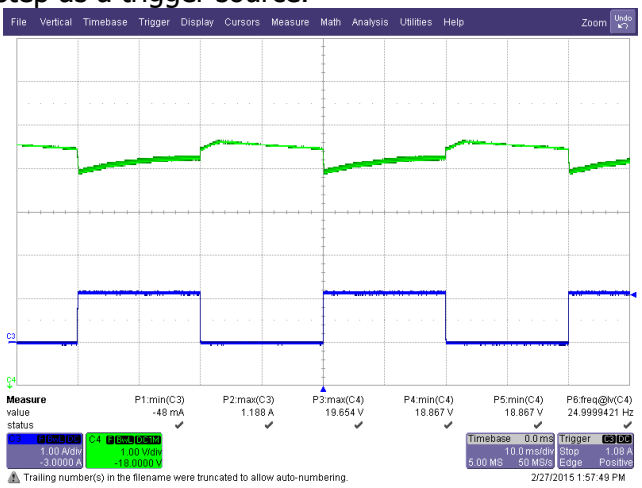

Figure 28 – Transient Response, 90 VAC, 0%<-->50% Step Load. Upper: V_{OUT}, 1 V / div. Lower: I_{OUT}, 1 A / div., 10 ms / div.

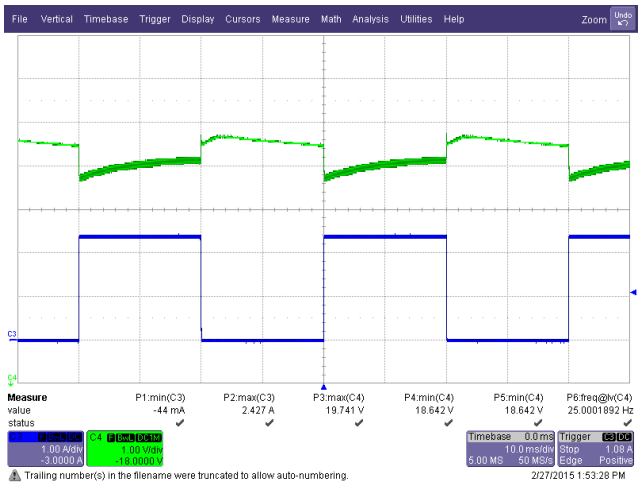

Figure 29 – Transient Response, 115 VAC, 0%<-->100% Step Load. Upper: V_{OUT}, 1.0 V / div. Lower: I_{OUT}, 1 A / div., 10 ms / div.

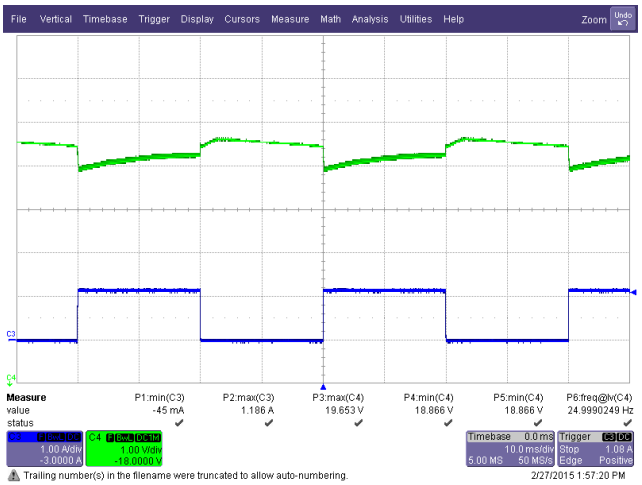

Figure 30 – Transient Response, 115 VAC, 0%<-->50% Step Load. Upper: V_{OUT}, 2.0 V / div. Lower: I_{OUT}, 1 A / div., 10 ms / div.

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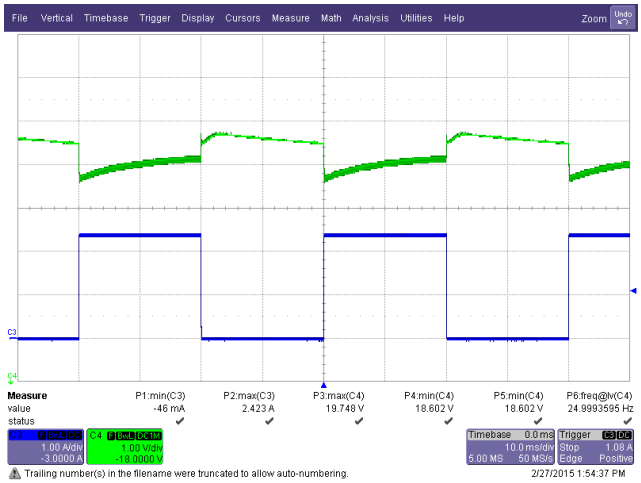

Figure 31 – Transient Response, 230 VAC, 0%<-->100% Step Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 1 A / div., 10 ms / div.

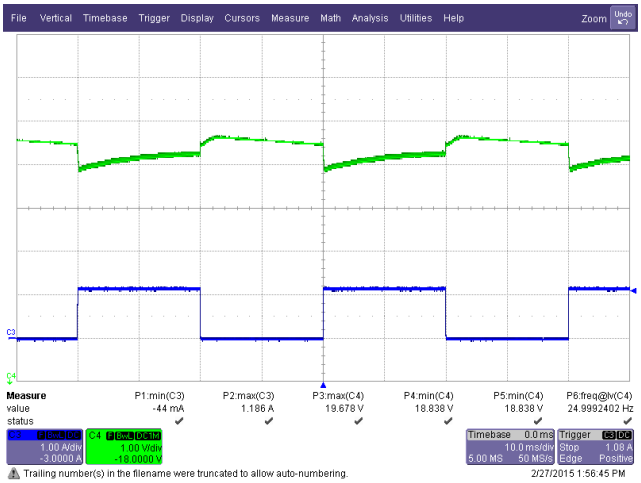

Figure 32 – Transient Response, 230 VAC, 0%<-->50% Step Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 1 A / div., 10 ms / div.

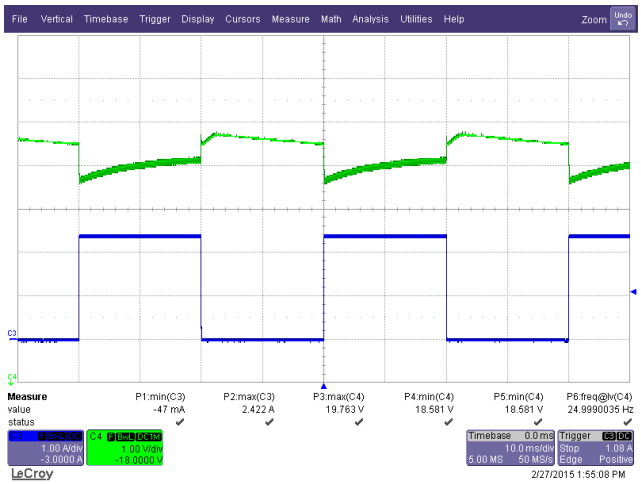

Figure 33 – Transient Response, 265 VAC, 0%<-->100% Step Load.
Upper: V_{OUT}, 1.0 V / div.
Lower: I_{OUT}, 1 A / div., 10 ms / div.

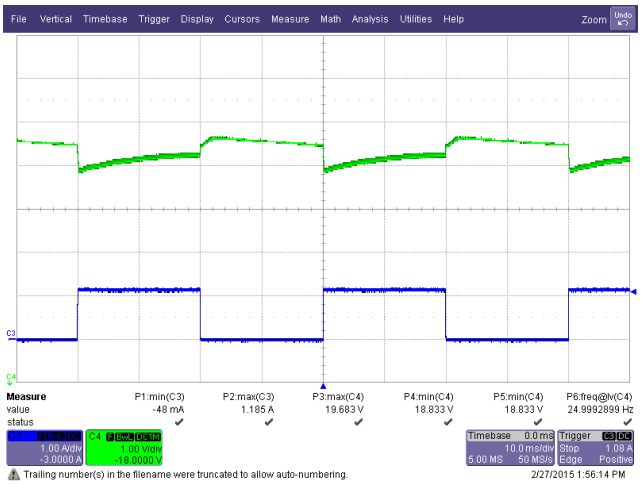

Figure 34 – Transient Response, 265 VAC, 0%<-->50% Step Load.
Upper: V_{OUT}, 2.0 V / div.
Lower: I_{OUT}, 1 A / div., 10 ms / div.

11.5 ***Output Voltage Start-Up***

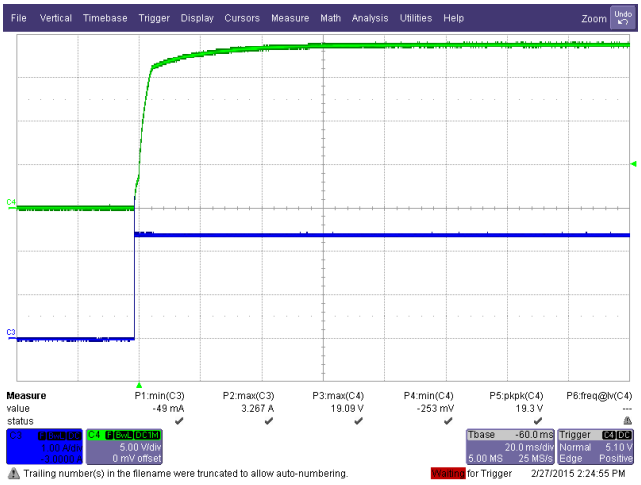

Figure 35 – Output Start-up. 90 VAC, Full Load.
Upper: 19 V V_{OUT}, 5 V / div.
Lower: 2.37 A I_{OUT}, 1 A / div., 20 ms / div.

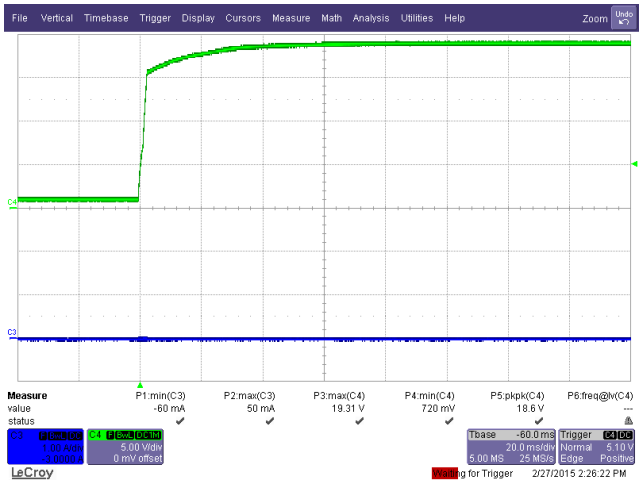

Figure 36 – Output Start-up. 90 VAC, No-Load.
Upper: 19 V V_{OUT}, 5 V / div.
Lower: 0 A I_{OUT}, 1 A / div., 20 ms / div.

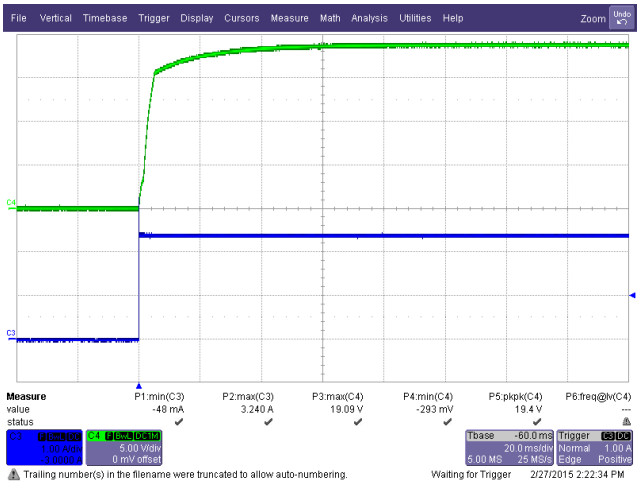

Figure 37 – Output Start-up. 115 VAC, Full Load.
Upper: 19 V V_{OUT}, 5 V / div.
Lower: 2.37 A I_{OUT}, 1 A / div., 20 ms / div.

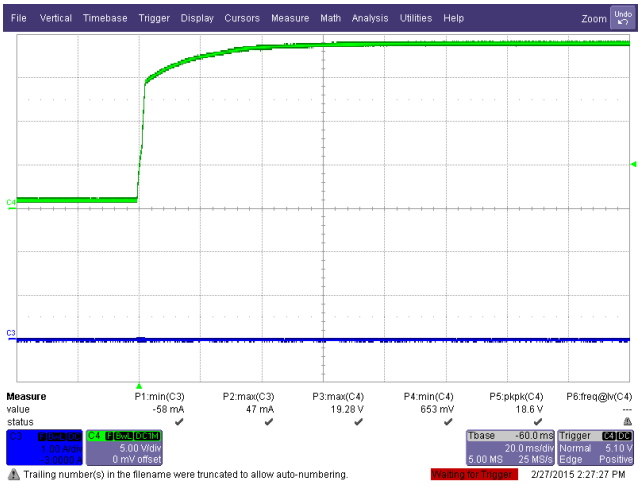

Figure 38 – Output Start-up. 115 VAC, No-Load.
Upper: 19 V V_{OUT}, 5 V / div.
Lower: 0 A I_{OUT}, 1 A / div., 20 ms / div.

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11.6 ***Output Rectifier Diode Voltage Waveforms***

Demonstrates 80% de-rating of 120 V diode rating

Figure 39 – 19 V Output rectifier diode voltage 100% Load, 265 VAC.
Upper: 120 V Output Diode PIV, 20 V / div., 2 µs / div.

11.7 ***Output Ripple and Noise Measurements***

11.7.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the figures below.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 1 μF / 50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

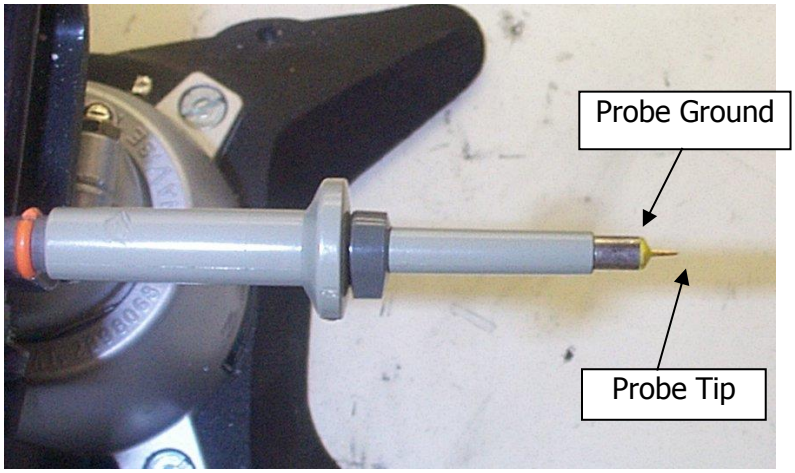

Figure 40 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

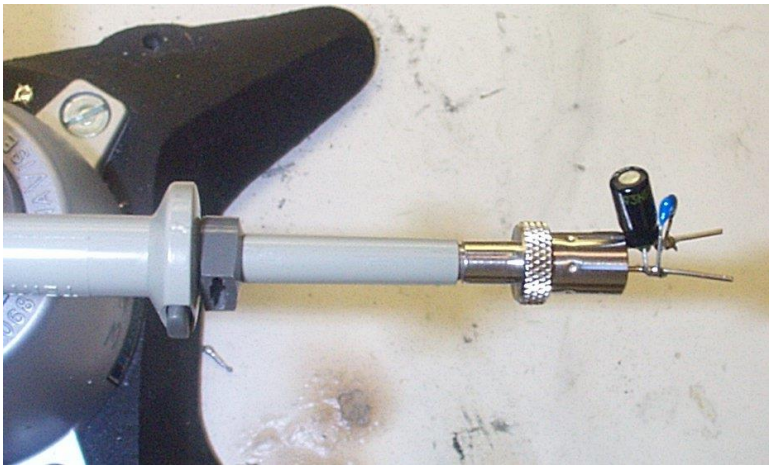

Figure 41 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with Wires for Probe Ground for Ripple Measurement, and Two Parallel Decoupling Capacitors Added).

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11.7.2 Ripple and Noise Measurement Results

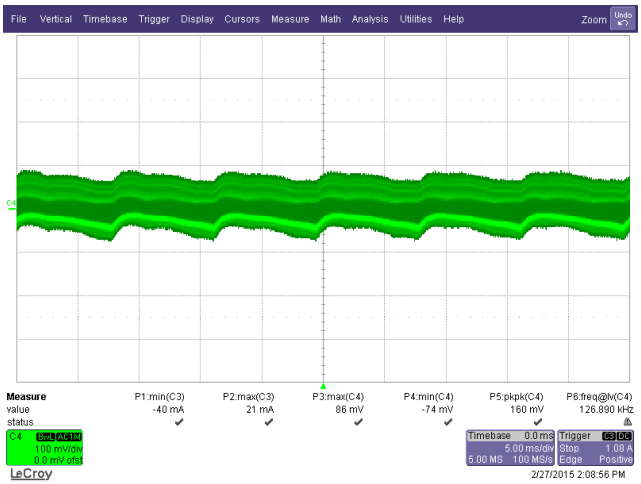

Figure 42 – Low Frequency Ripple, 90 VAC, Full Load. V_{OUT}, 100 mV / div. 5 ms / div.

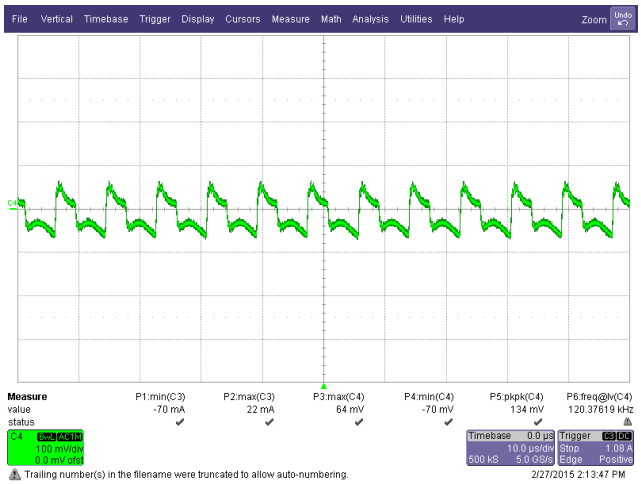

Figure 43 – Switching Noise, 90 VAC, Full Load. V_{OUT}, 100 mV / div. 10 μs / div.

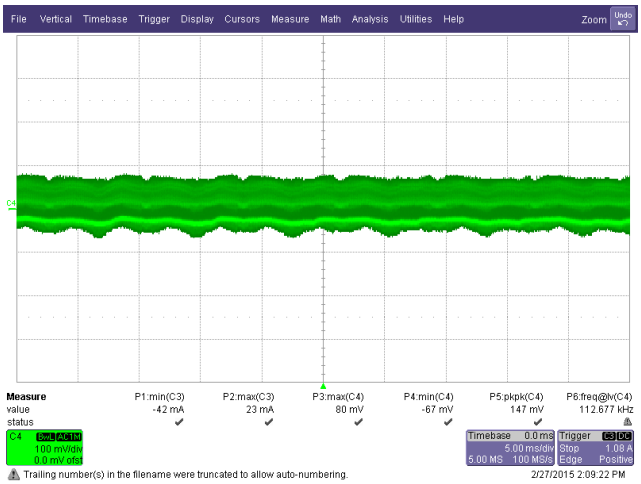

Figure 44 – Low Frequency Ripple, 115 VAC, Full Load. V_{OUT}, 100 mV / div. 5 ms / div.

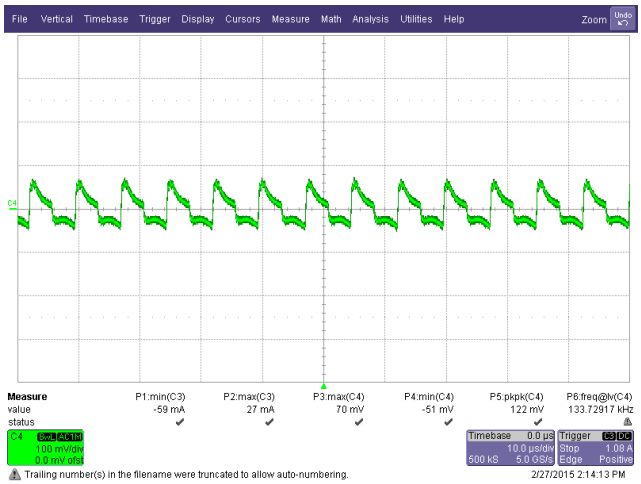

Figure 45 – Switching Noise, 115 VAC, Full Load. V_{OUT}, 100 mV / div. 10 μs / div.

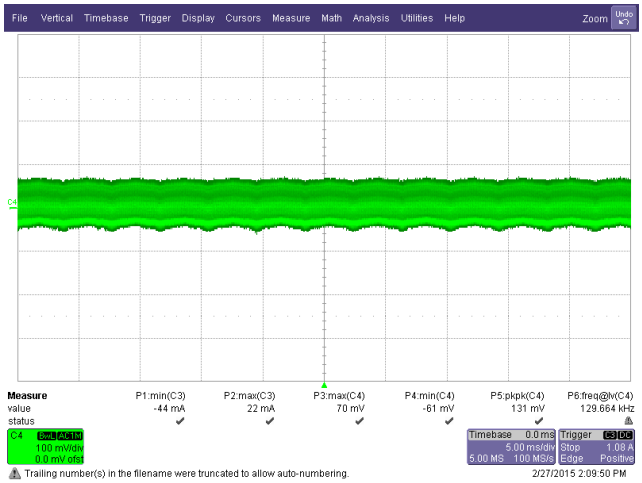

Figure 46 – Low Frequency Ripple, 230 VAC, Full Load. V_{OUT}, 100 mV / div. 5 ms / div.

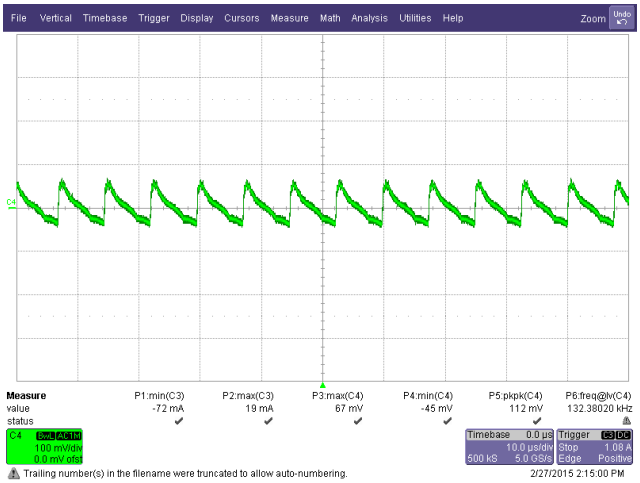

Figure 47 – Switching Noise, 230 VAC, Full Load. V_{OUT}, 100 mV / div. 10 µs / div.

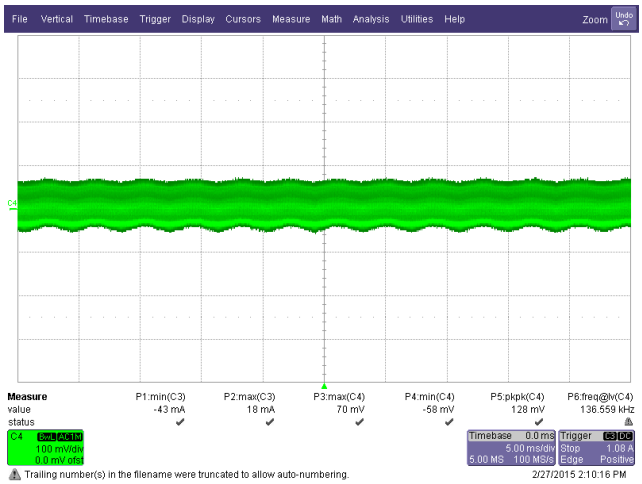

Figure 48 – Low Frequency Ripple, 265 VAC, Full Load. V_{OUT}, 100 mV / div. 5 ms / div.

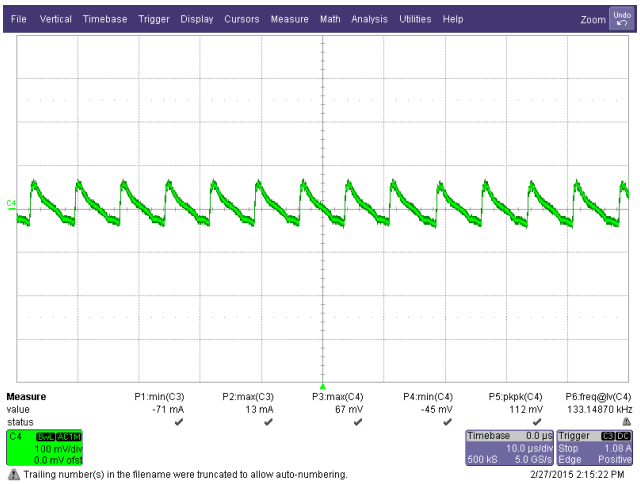

Figure 49 – Switching Noise, 265 VAC, Full Load. V_{OUT}, 100 mV / div. 10 µs / div.

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12 Thermal Performance

12.1 *Thermal Performance ($T_{AMBIENT}$ = 25 °C)*

Thermal performance was measured at full load operation, open frame at ambient temperature of 25 °C. The transformer winding temperature was taken on the outermost layer.

Item	Description	100 VAC Full Load (ºC)
1	Output Diode (D4)	77.9
2	Output Diode Heat Sink (HS2)	74.1
3	Secondary Snubber Resistor (R19, R20)	75.7
4	Output Capacitor (C15)	52.8
5	LNK6777E (U1)	73.3
6	LNK6777E Heat Sink (HS1)	69.3
7	Transformer Winding (T1)	80.2
8	NTC (RT1)	79.1
9	Input Capacitor (C9)	52.9
10	Input CMC (L2)	57.6
11	Bridge Rectifier (BR1)	74.5
12	Primary Clamp Resistor (R1, R2, R3)	72.1

12.2 *Thermal Performance ($T_{AMBIENT}$ = 45 °C)*

Thermal performance was measured at full load operation, enclosed in a box and placed inside a thermal chamber at ambient temperature of 45°C. The transformer winding temperature was taken on the outermost layer.

Item	Description	100 VAC Full Load (ºC)	90 VAC Full Load (ºC)
1	Output Diode (D4)	108.3	111.8
2	Secondary Snubber Resistor (R19, R20)	98.1	101.1
3	Primary Clamp Diode (D1)	99.6	103.9
4	Primary Clamp Resistor (R1, R2, R3)	101.9	106.4
5	LNK6777E (U1)	100.8	106.9
6	Transformer Winding (T1)	106	110.5
7	Transformer Core (T1)	103.3	107.5
8	Bridge Rectifier (BR1)	99	105.8
9	Ambient Inside the Box	71.8	74.4

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13 Gain-Phase Measurement

13.1 *Gain-Phase Plot*

Gain-phase measurements were carried out on DER-581 at 20%, 50% and 100% loads.

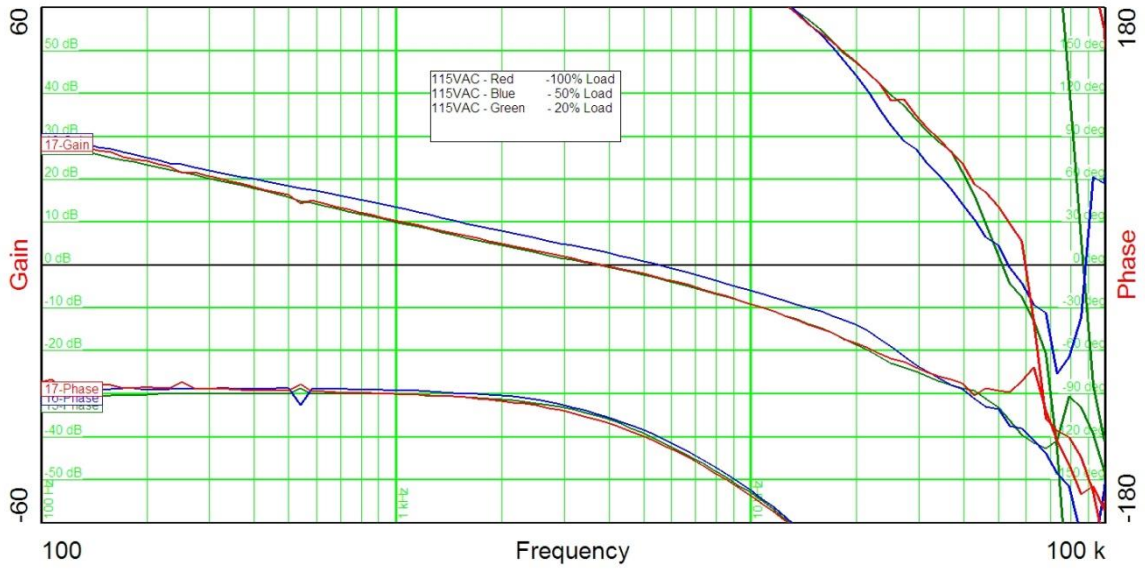

Figure 83 – Gain-Phase Measurement at 115 VAC Input.

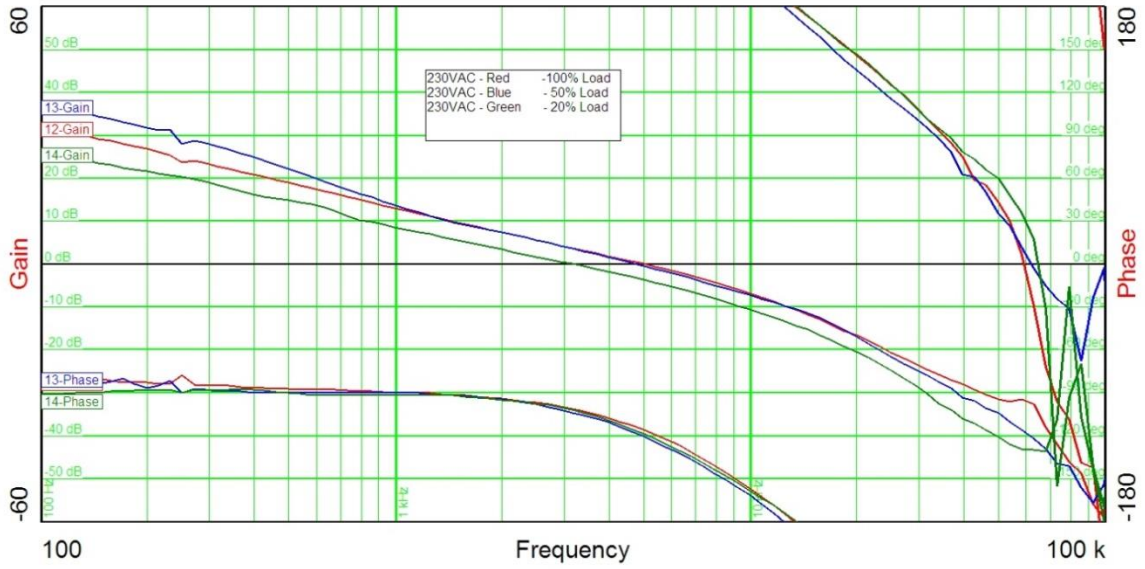

Figure 83 – Gain-Phase Measurement at 230 VAC Input.

14 AC Surge (Resistive Full Load at the Output)

Following Common mode and differential mode surge tests were performed on DER-581 power supply. 10 strikes have been applied on each condition.

Combination Wave Surge Test (IEC 61000-4-5)							
S/N	**Polarity**	**Voltage (kV)**	**Time Interval**	**Impedance (Ω)**	**Angle**	**Common Mode**	**Test Result**
1	Positive	3	10 Sec	12	0, 90, 180 & 270 Deg	L, N-PE	Pass
2	Negative	3	10 Sec	12	0, 90, 180 & 270 Deg	L, N-PE	Pass
3	Positive	3	10 Sec	12	0, 90, 180 & 270 Deg	L-PE	Pass
4	Negative	3	10 Sec	12	0, 90, 180 & 270 Deg	L-PE	Pass
5	Positive	3	10 Sec	12	0, 90, 180 & 270 Deg	N-PE	Pass
6	Negative	3	10 Sec	12	0, 90, 180 & 270 Deg	N-PE	Pass

Combination Wave Surge Test (IEC 61000-4-5)							
S/N	**Polarity**	**Voltage (kV)**	**Time Interval**	**Impedance (Ω)**	**Angle**	**Differential Mode**	**Test Result**
1	Positive	3	10 Sec	2	0, 90, 180 & 270 Deg	L-N	Pass
2	Negative	3	10 Sec	2	0, 90, 180 & 270 Deg	L-N	Pass

Electrical Fast Transient Burst Test (IEC 61000-4-4)								
S/N	**# of Pulses**	**Voltage (kV)**	**Duration**	**Repetition Frequency**	**Angle**	**CM/DM**	**Repetitive Bursts**	**Test Result**
1	75	±2	1 Min	2.5 kHz ± 20%	Asynchronous	L, N, PE	300 ms	Pass
2	75	±2	1 Min	2.5 kHz ± 20%	Asynchronous	L, N	300 ms	Pass

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15 ESD (Resistive Full Load at the Output)

Device	Discharge Type	Discharge Location	Voltage (kV)	# of Events (1 / Sec)	Remarks
LNK6777E	Contact	+ Output Terminal	+8.8	10	PASS
			-8.8	10	PASS
		- Output Terminal	+8.8	10	PASS
			-8.8	10	PASS
	Air	+ Output Terminal	+16.5	10	PASS
			-16.5	10	PASS
		- Output Terminal	+16.5	10	PASS
			-16.5	10	PASS

PASS = No output glitch or latch-off.

16 EMI Tests at Full Load

Conducted and radiated emissions tests were performed at 115 VAC and 230 VAC at full load. Composite EN55022B / CISPR22B conducted limits are shown. All the tests show excellent EMI performance.

16.1 *Conducted EMI Test Set-Up*

Note:

1. Copper foil with insulation was used to wrap the board and copper foil was connected to secondary ground.
2. Ferrite beads (Qty-2) were used on output cable (King core P/N: K5BT14.2*13.5*6.35).

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16.2 *Conducted EMI Results*

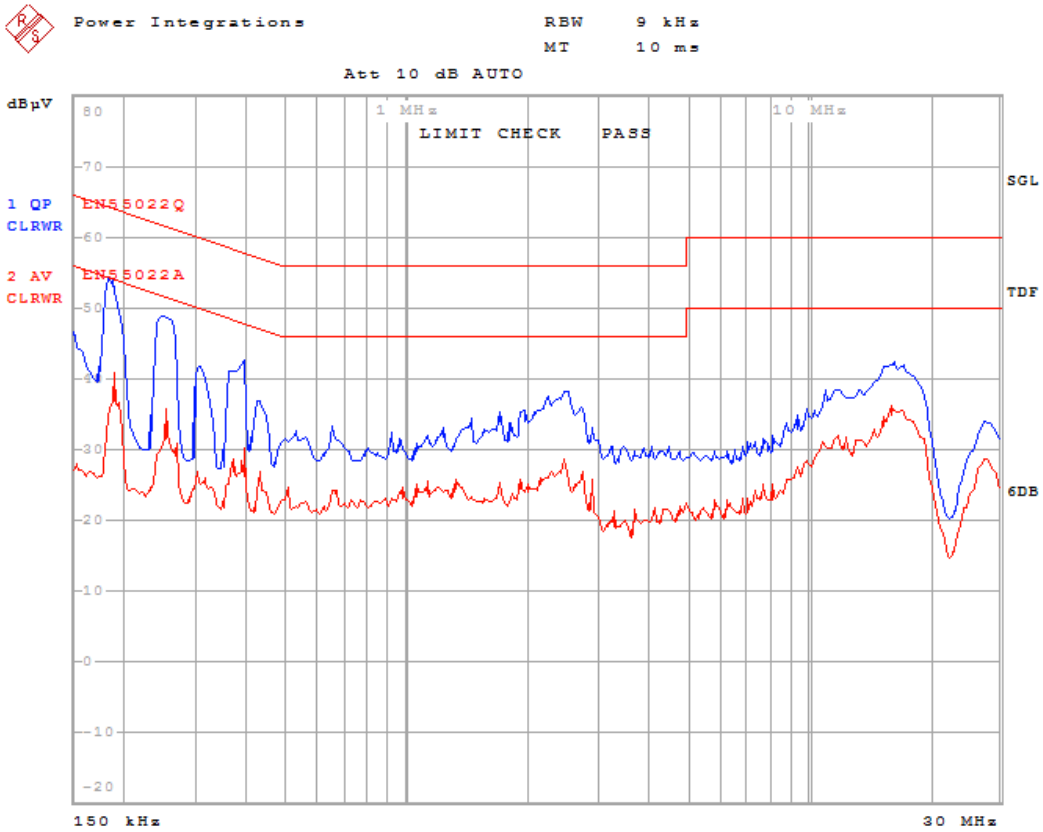

Figure 50 – Conducted EMI plot at 115 VAC 60 Hz, Full Load (Grounded Secondary).

EDIT PEAK LIST (Prescan Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	150 kHz	46.31	N gnd	-19.68
1	Quasi Peak	182.849162999 kHz	54.48	N gnd	-9.87
2	Average	190.236269184 kHz	40.03	N gnd	-13.99
1	Quasi Peak	251.012717153 kHz	50.17	N gnd	-11.55
2	Average	251.012717153 kHz	39.45	N gnd	-12.26
1	Quasi Peak	305.983101557 kHz	42.02	N gnd	-18.05
1	Quasi Peak	372.991693411 kHz	43.10	N gnd	-15.32
2	Average	388.060557825 kHz	30.64	N gnd	-17.46
1	Quasi Peak	428.450212374 kHz	37.95	N gnd	-19.33
2	Average	1.46255097494 MHz	31.83	N gnd	-14.16
1	Quasi Peak	1.74788380138 MHz	42.79	N gnd	-13.20
2	Average	2.21673928895 MHz	32.28	N gnd	-13.71
1	Quasi Peak	2.26107407473 MHz	42.67	N gnd	-13.32
1	Quasi Peak	17.0424610519 MHz	48.50	N gnd	-11.49
2	Average	17.3833102729 MHz	42.24	N gnd	-7.75

Figure 51 – Conducted EMI limits at 115 VAC 60 Hz, Full Load (Grounded Secondary).

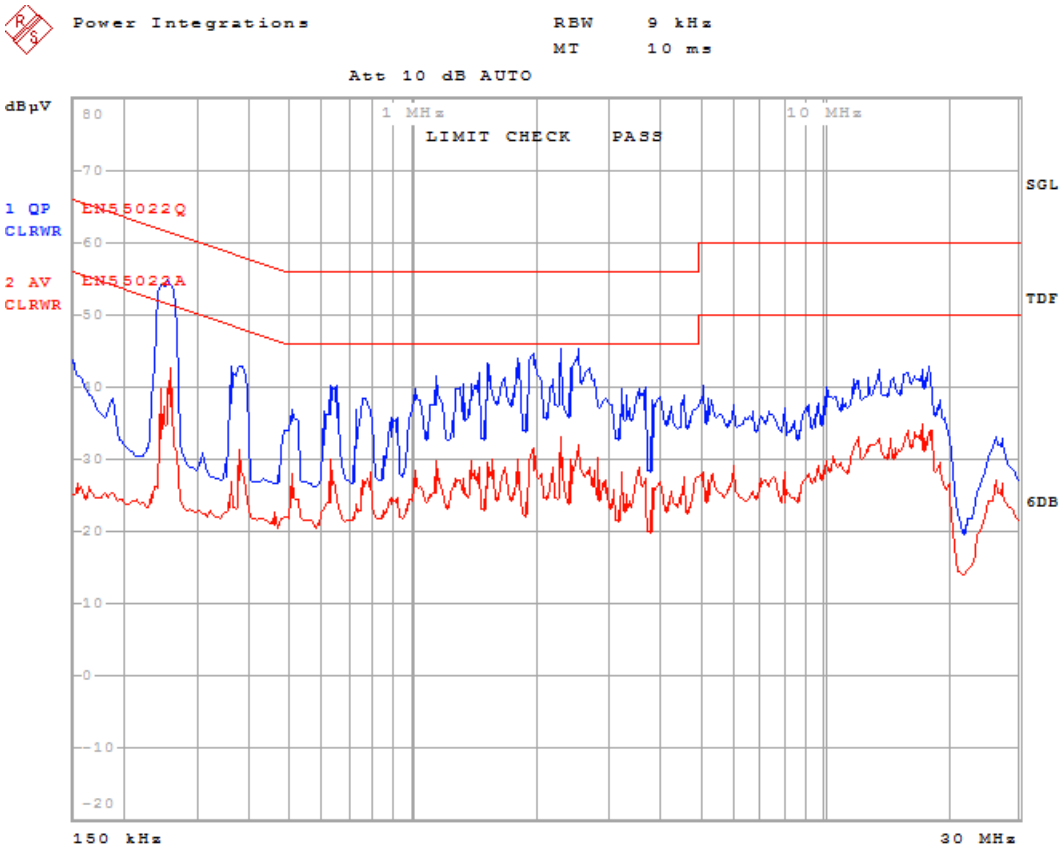

Figure 52 – Conducted EMI plot at 230 VAC 60 Hz, Full Load (Grounded Secondary).

EDIT PEAK LIST (Prescan Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	256.032971496 kHz	55.06	N gnd	-6.49
2	Average	261.153630926 kHz	42.65	N gnd	-8.73
1	Quasi Peak	380.451527279 kHz	42.98	N gnd	-15.28
2	Average	380.451527279 kHz	31.24	N gnd	-17.02
2	Average	636.654477383 kHz	29.91	N gnd	-16.08
1	Quasi Peak	1.15321146268 MHz	41.54	N gnd	-14.45
2	Average	1.15321146268 MHz	29.73	N gnd	-16.26
2	Average	1.40575833808 MHz	29.73	N gnd	-16.26
1	Quasi Peak	1.46255097494 MHz	42.02	N gnd	-13.97
1	Quasi Peak	1.52163803433 MHz	43.44	N gnd	-12.55
2	Average	1.58311221091 MHz	30.08	N gnd	-15.91
1	Quasi Peak	1.81849830696 MHz	43.92	N gnd	-12.07
1	Quasi Peak	1.96840105035 MHz	44.63	N gnd	-11.36
2	Average	1.96840105035 MHz	31.70	N gnd	-14.29
1	Quasi Peak	2.30629555622 MHz	45.15	N gnd	-10.84
2	Average	2.30629555622 MHz	33.03	N gnd	-12.96
1	Quasi Peak	2.54633665013 MHz	45.16	N gnd	-10.83
2	Average	2.54633665013 MHz	32.01	N gnd	-13.98
2	Average	17.3833102729 MHz	35.01	N gnd	-14.98
1	Quasi Peak	18.085596008 MHz	42.74	N gnd	-17.25

Figure 53 – Conducted EMI limits at 230 VAC 60 Hz, Full Load (Grounded Secondary).

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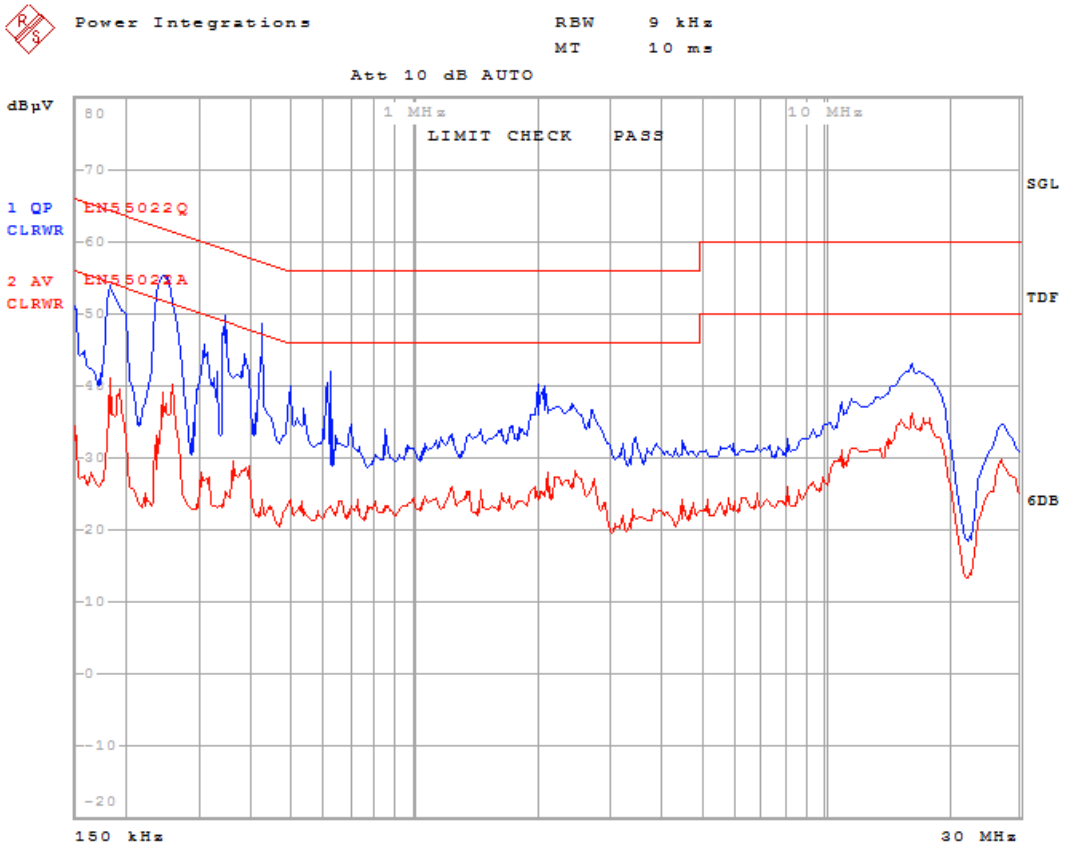

Figure 54 – Conducted EMI plot at 115 VAC 60 Hz, Full Load (Floating Secondary).

EDIT PEAK LIST (Prescan Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	150 kHz	50.88	N gnd	-15.11
1	Quasi Peak	182.849162999 kHz	53.80	N gnd	-10.55
2	Average	182.849162999 kHz	40.99	N gnd	-13.36
1	Quasi Peak	251.012717153 kHz	55.30	N gnd	-6.41
2	Average	261.153630926 kHz	40.22	N gnd	-11.16
1	Quasi Peak	312.102763589 kHz	45.62	N gnd	-14.28
1	Quasi Peak	351.478403302 kHz	49.56	N gnd	-9.36
2	Average	365.678130795 kHz	29.35	N gnd	-19.24
1	Quasi Peak	428.450212374 kHz	48.56	N gnd	-8.71
1	Quasi Peak	501.99771062 kHz	39.91	N gnd	-16.08
1	Quasi Peak	624.171056258 kHz	42.05	N gnd	-13.94
1	Quasi Peak	2.00776907136 MHz	40.25	N gnd	-15.74
2	Average	2.49640848052 MHz	28.26	N gnd	-17.73
1	Quasi Peak	16.3806815186 MHz	43.05	N gnd	-16.94
2	Average	16.3806815186 MHz	36.21	N gnd	-13.78

Figure 55 – Conducted EMI limits at 115 VAC 60 Hz, Full Load (Floating Secondary).

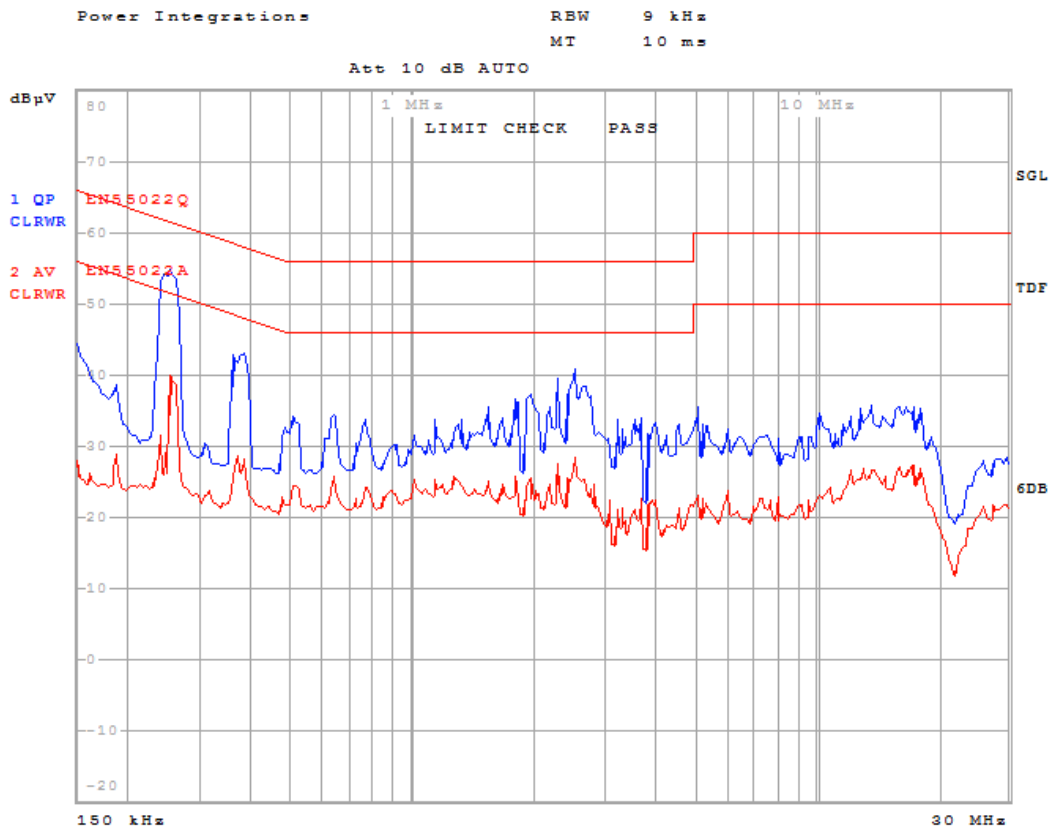

Figure 56 – Conducted EMI plot at 230 VAC 60 Hz, Full Load (Floating Secondary).

EDIT PEAK LIST (Prescan Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	256.032971496 kHz	54.81	N gnd	-6.74
2	Average	256.032971496 kHz	40.07	N gnd	-11.48
2	Average	372.991693411 kHz	28.78	N gnd	-19.65
1	Quasi Peak	388.060557825 kHz	43.07	N gnd	-15.03
1	Quasi Peak	1.81849830696 MHz	36.43	N gnd	-19.56
1	Quasi Peak	1.96840105035 MHz	37.43	N gnd	-18.56
1	Quasi Peak	2.30629555622 MHz	39.39	N gnd	-16.61
2	Average	2.30629555622 MHz	27.53	N gnd	-18.46
1	Quasi Peak	2.54633665013 MHz	40.71	N gnd	-15.28
2	Average	2.54633665013 MHz	28.39	N gnd	-17.60

Figure 57 – Conducted EMI limits at 230 VAC 60 Hz, Full Load (Floating Secondary).

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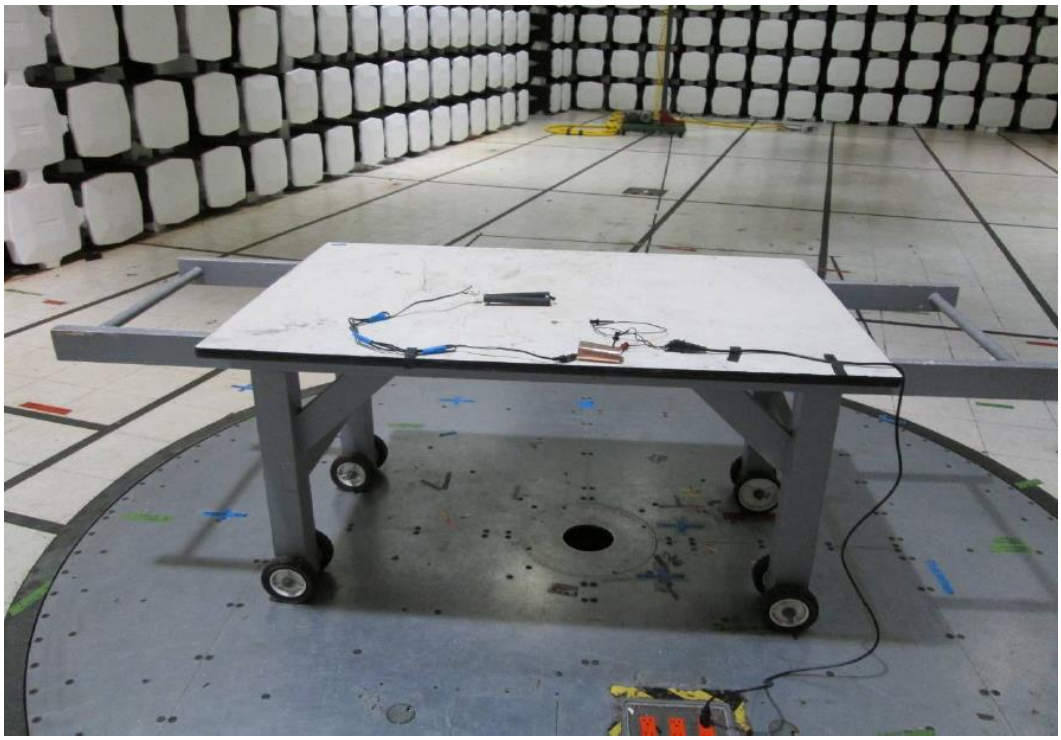
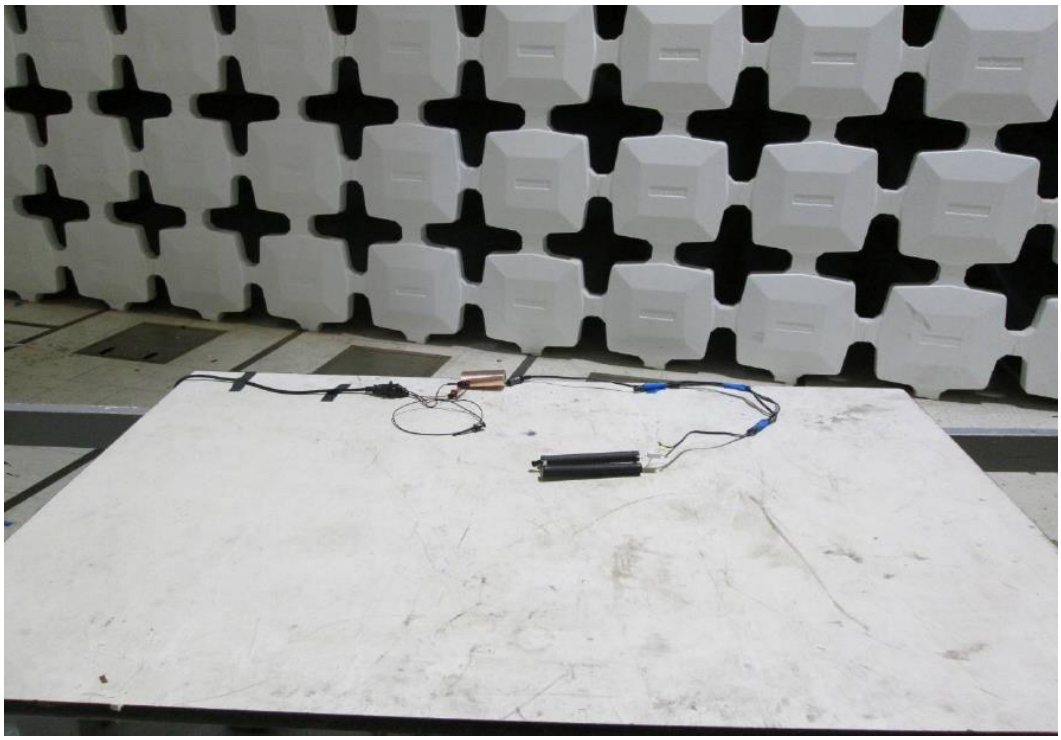
16.3 ***Radiated EMI Test Set-Up***





16.4 *Radiated EMI Results (Vertical Only up to 3 M)*

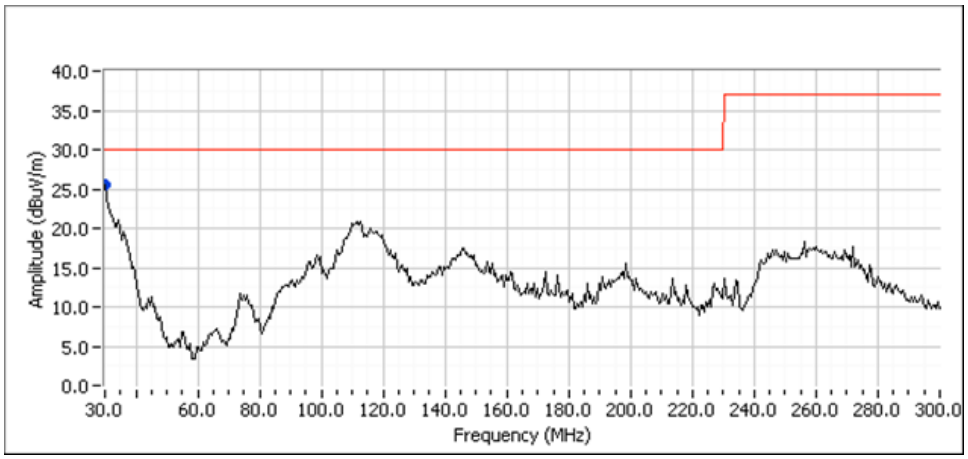


Figure 58 – Radiated EMI Peak Plot at 110 VAC 60 Hz, Full Load (Floating Secondary).

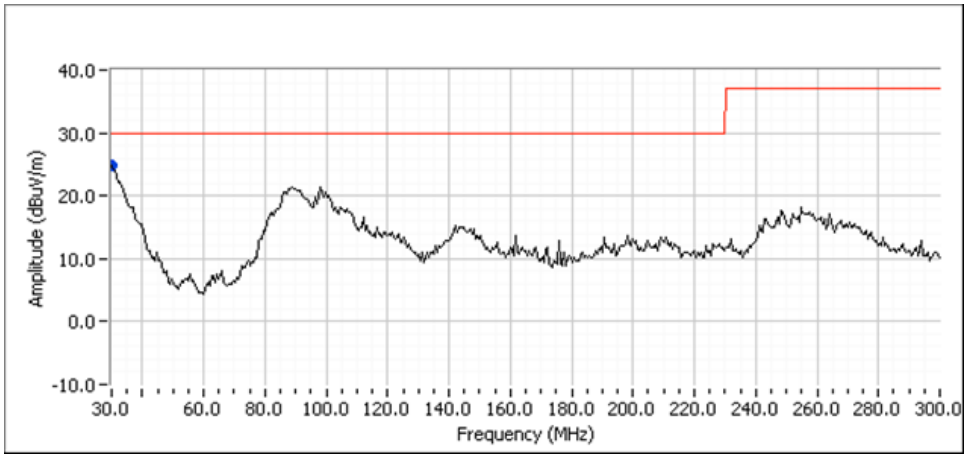


Figure 59 – Radiated EMI Peak Plot at 110 VAC 60 Hz, Full Load (Grounded Secondary).

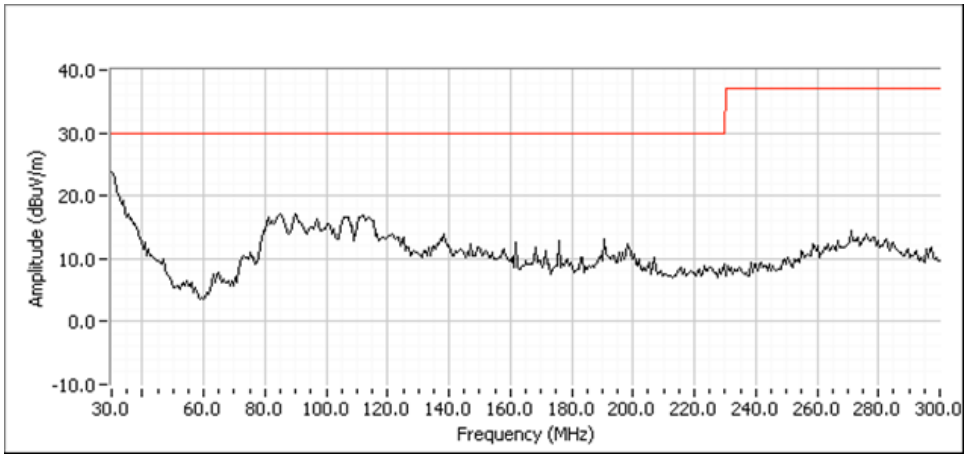


Figure 60 – Radiated EMI Peak Plot at 230 VAC 50 Hz, Full Load (Floating Secondary).

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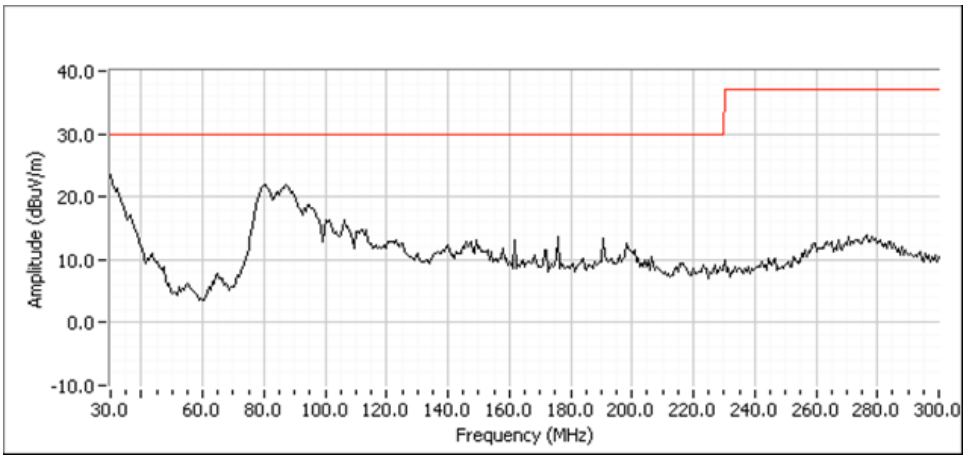

Figure 61 – Radiated EMI Peak Plot at 110 VAC 60 Hz, Full Load (Grounded Secondary).

17 Revision History

Date	Author	Revision	Description and Changes	Reviewed
11-Oct-16	SS	1.0	Initial Release.	Apps & Mktg
07-Feb-17	KM	1.1	Added Magnetics Supplier	

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@power.com

GERMANY
Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@power.com

JAPAN
Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@power.com

UK
First Floor, Unit 15, Meadway
Court, Rutherford Close,
Stevenage, Herts. SG1 2EF
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail: eurosales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
Fax: +86-755-8672-8690
e-mail: chinasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni
(MI) Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@power.com