Q100 Qualification Test Plan

Automotive Grade Level = 1 -40 to +125C MSL = 3

Supplier Name:	Power Integrations		**General Specification:**	AEC-Q100 Rev. H	
Supplier Code:	N/A		**Supplier Wafer Fabrication:**	Lapis S2 (Miyagi, Japan)	
Supplier Part Number:	INN3977CQ		**Supplier Wafer Test:**	N/A	
Supplier Contact:	Edward Ong		**Supplier Assembly Site:**	Hana (Ayutthaya, Thailand)	
Supplier Family Type:	Integrated Circuit		**Supplier Final Test Site:**	Hana (Ayutthaya, Thailand)	
Device Description:	CV/CC QR Flyback Switcher IC		**Supplier Reliability Signature:**	Nick Stanco	
PPAP Submission Date:	TBD		**Customer Test ID:**	N/A	
Reason for Qualification:	New Part Qualification		**Customer Part Number:**	N/A	
Prepared by Signature:	Joseph Ho	Date: 05/03/20	**Customer Approval Signature:**	N/A	Date:N/A

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS								
PC	A1	JESD22 A113 J-STD-020	Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for THB/HAST, AC/UHST, TC, & PTC; Peak Reflow Temp = 260°C	Min. MSL = 3			MSL = 3	
THB or HAST	A2	JESD22 A101 JESD22 A110	Temperature Humidity Bias: (Test @ Rm/Hot) 85°C / 85%R.H.; 1000 hours; Vd = 30V Highly Accelerated Stress Test: (Test @ Rm/Hot/)	3	77	231	1 of 231	THB 1000 hours had 1 unit fail BPP pin continuity due to non-optimized wire bonding. Corrective action has been identified and will be implemented prior to shipment to customers.
AC or UHST or TH	A3	JESD22 A102 JESD22 A118 or JESD22-A101	Autoclave: (Test @ Rm) Unbiased Highly Accelerated Stress Test: (Test @ Rm) Temperature Humidity without Bias: (Test @ Rm) 130°C / 85%R.H.; 96 hours	3	77	231	0 of 231	
TC	A4	JESD22 A104	Temperature Cycle: (Test @ Hot) -40°C to +125°C; 1700 Cycles	3	77	231	0 of 231	
PTC	A5	JESD22 A105	Power Temperature Cycle: (Test @ Rm/Hot) -40°C to +125°C; 1000 Cycles	1	45	45	0 of 45	
HTSL	A6	JESD22 A103	High Temperature Storage Life: (Test @ Rm/Hot) 150°C; 1000 Hours	1	45	45	0 of 45	

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS								
HTOL	B1	JESD22 A108	High Temp Operating Life: (Test @ Rm/Cold/Hot) Tj = 125°C; 1000 hours; Vd = 600V	3	77	231	0 of 231	
ELFR	B2	AEC-Q100-008	Early Life Failure Rate: (Test @ Rm/Hot) Tj = 125°C; 48 hours; Vd = 600V	3	800	2400	0 of 2400	
EDR	B3	AEC-Q100-005	NVM Endurance & Data Retention Test: (Test @ Rm/Hot)	3	77	231	of	N/A
TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS								
WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear Test: (Cpk > 1.67)	30 bonds	5 parts Min.	180 bonds	0 of 180	
WBP	C2	Mil-STD-883, Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30 bonds	5 parts Min.	180 bonds	0 of 180	
SD	C3	JESD22 B102 JSTD-002D	Solderability: (>95% coverage) 8hr steam aging prior to testing	1	15	15	0 of 15	
PD	C4	JESD22 B100, JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	3	10	30	0 of 30	
SBS	C5	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices	3	50 balls		of	N/A
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through-hole only; 10 leads from each of 5 devices	1	50 leads		of	N/A
TEST GROUP D – DIE FABRICATION RELIABILITY TESTS								
EM	D1	JESD61	Electromigration:	-	-	-	0	Data Available 3 lots performed by Lapis S2; Total of 51 chips.
TDDB	D2	JESD35	Time Dependant Dielectric Breakdown:	-	-	-	0	Data Available 1 lot performed by Lapis S2; Total of 432 chips.
HCI	D3	JESD60 & 28	Hot Carrier Injection:	-	-	-	0	Data Available 3 lots performed by Lapis S2; Toal of 90 chips for LV and 125 chips for MV.

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
NBTI	D4	JESD90	Negative Bias Temperature Instability:	-	-	-	0	Data Available 1 lot performed by Lapis S2; Total of 15 chips.
SM	D5	JESD61, 87, & 202	Stress Migration:	-	-	-	0	Data Available 5 lots performed by Lapis S2; Total of 318 chips.

TEST GROUP E- ELECTRICAL VERIFICATION

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test:	All	All	All	1 of All	See A2 - THB
HBM	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model: (Test @ Rm/Hot); (2KV HBM / Class 2 or better)	1	12	12	0 of 12 ESD Level = 2	Passed 500V, 1KV, 1.5KV, 2KV
CDM	E3	AEC-Q100-011	Electrostatic Discharge, Charged Device Model: (Test @ Rm/Hot); (750V corner leads, 500V all other leads / Class C4B or better)	1	12	12	0 of 12 ESD Level = C3	Passed 250V, 500V, 750V, 1KV
LU	E4	AEC-Q100-004	Latch-Up: (Test @ Rm/Hot) +125C	1	6	6	0 of 6	
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (where applicable, Cpk >1.67)	3	30	90	0 of 90	
FG	E6	AEC-Q100-007	Fault Grading:	-	-	-	Fault Grade Other (explain)	Substituting 100% functional coverage
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-	PPAP Data	
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1	1	1		Estimated Completion Date = June 2020; Non-Gating requirement.
SC	E10	AEC Q100-012	Short Circuit Characterization	3	10	30		N/A
SER	E11	JESD89-1 JESD89-2 JESD89-3	Soft Error Rate	1	3	3		N/A
LF	E12	AEC-Q005	Lead (Pb) Free: (see AEC-Q005)	-	-	-	Done	Passed

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
TEST GROUP F – DEFECT SCREENING TESTS								
PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	All	All	All	Reject units outside Avg.	
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)	All	All	All	Reject units outside criteria	
TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS (for Ceramic Package testing only)								
MS	G1	JESD22 B104	Mechanical Shock: (Test @ Rm)	1	15	15	of	N/A
VFV	G2	JESD22 B103	Variable Frequency Vibration: (Test @ Rm)	1	15	15	of	N/A
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration: (Test @ Rm)	1	15	15	of	N/A
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak:	1	15	15	of	N/A
DROP	G5	----------	Drop Test: (Test @ Rm) MEMS cavity parts only. Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.	1	5	5	of	N/A
LT	G6	MIL-STD-883 Method 2004	Lid Torque:	1	5	5	of	N/A
DS	G7	MIL-STD-883 Method 2019	Die Shear:	1	5	5	of	N/A
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor:	1	3	3	of	N/A

Q100 Qualification Test Plan

Automotive Grade Level = 1 -40 to +125C MSL = 3

Supplier Name:	Power Integrations		**General Specification:**	AEC-Q100 Rev. H	
Supplier Code:	N/A		**Supplier Wafer Fabrication:**	Lapis (Miyagi, Japan)	
Supplier Part Number:	INN3996CQ		**Supplier Wafer Test:**	N/A	
Supplier Contact:	Edward Ong		**Supplier Assembly Site:**	Hana (Ayutthaya, Thailand)	
Supplier Family Type:	Integrated Circuit		**Supplier Final Test Site:**	Hana (Ayutthaya, Thailand)	
Device Description:	CV/CC QR Flyback Switcher IC		**Supplier Reliability Signature:**	Nick Stanco	
PPAP Submission Date:	TBD		**Customer Test ID:**	N/A	
Reason for Qualification:	New Part Qualification		**Customer Part Number:**	N/A	
Prepared by Signature:	Joseph Ho	Date: 12/30/20	**Customer Approval Signature:**	N/A	Date:N/A

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS								
PC	A1	JESD22 A113 J-STD-020	Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for THB/HAST, AC/UHST, TC, & PTC; Peak Reflow Temp = 260°C	Min. MSL = 3			MSL = 3	
THB or HAST	A2	JESD22 A101 JESD22 A110	Temperature Humidity Bias: (Test @ Rm/Hot) 85°C / 85%R.H.; 1000 hours; Vd = 30V Highly Accelerated Stress Test: (Test @ Rm/Hot/)	1	77	77	0 of 77	
AC or UHST or TH	A3	JESD22 A102 JESD22 A118 or JESD22-A101	Autoclave: (Test @ Rm) Unbiased Highly Accelerated Stress Test: (Test @ Rm) Temperature Humidity without Bias: (Test @ Rm) 130°C / 85%R.H.; 96 hours	1	77	77	0 of 77	
TC	A4	JESD22 A104	Temperature Cycle: (Test @ Hot) -40°C to +125°C; 1700 Cycles	1	77	77	0 of 77	
PTC	A5	JESD22 A105	Power Temperature Cycle: (Test @ Rm/Hot) -40°C to +125°C; 1000 Cycles	1	45	45	0 of 45	
HTSL	A6	JESD22 A103	High Temperature Storage Life: (Test @ Rm/Hot) 150°C; 1000 Hours	1	45	45	0 of 45	

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS								
HTOL	B1	JESD22 A108	High Temp Operating Life: (Test @ Rm/Cold/Hot) Tj = 125°C; 1000 hours; Vd = 720V	1	77	77	0 of 77	
ELFR	B2	AEC-Q100-008	Early Life Failure Rate: (Test @ Rm/Hot) Tj = 125°C; 48 hours; Vd = 720V	1	800	800	0 of 800	
EDR	B3	AEC-Q100-005	NVM Endurance & Data Retention Test: (Test @ Rm/Hot)	1	77	-	of	N/A
TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS								
WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear Test: (Cpk > 1.67)	30 bonds	5 parts Min.	180 bonds	0 of 180	Generic Data applied (see INN3977CQ)
WBP	C2	Mil-STD-883, Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30 bonds	5 parts Min.	180 bonds	0 of 180	Generic Data applied (see INN3977CQ)
SD	C3	JESD22 B102 JSTD-002D	Solderability: (>95% coverage) 8hr steam aging prior to testing	1	15	15	0 of 15	
PD	C4	JESD22 B100, JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	1	10	10	0 of 10	
SBS	C5	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices	-	50 balls		of	N/A
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through-hole only; 10 leads from each of 5 devices	-	50 leads		of	N/A
TEST GROUP D – DIE FABRICATION RELIABILITY TESTS								
EM	D1	JESD61	Electromigration:	-	-	-	0	Data Available 3 Total of 51 chips from 3 lots.
TDDB	D2	JESD35	Time Dependant Dielectric Breakdown:	-	-	-	0	Data Available Total of 432 chips from 1 lot.
HCI	D3	JESD60 & 28	Hot Carrier Injection:	-	-	-	0	Data Available Total of 90 chips for LV and 125 chips for MV from 3 lots.

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
NBTI	D4	JESD90	Negative Bias Temperature Instability:	-	-	-	0	Data Available Total of 15 chips from 1 lot.
SM	D5	JESD61, 87, & 202	Stress Migration:	-	-	-	0	Data Available Total of 318 chips from 5 lots.

TEST GROUP E- ELECTRICAL VERIFICATION

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test:	All	All	All	1 of All	
HBM	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model: (Test @ Rm/Hot); (2KV HBM / Class 2 or better)	1	12	12	0 of 12 ESD Level = 2	Passed 500V, 1KV, 1.5KV, 2KV
CDM	E3	AEC-Q100-011	Electrostatic Discharge, Charged Device Model: (Test @ Rm/Hot); (750V corner leads, 500V all other leads / Class C4B or better)	1	12	12	0 of 12 ESD Level = C3	Passed 250V, 500V, 750V, 1KV
LU	E4	AEC-Q100-004	Latch-Up: (Test @ Rm/Hot) +125C	1	6	6	0 of 6	
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (where applicable, Cpk >1.67)	3	30	90	0 of 90	
FG	E6	AEC-Q100-007	Fault Grading:	-	-	-	Fault Grade Other (explain)	Substituting 100% functional coverage
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-	PPAP Data	
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1	1	1	0	Completed. Data avaialble upon request.
SC	E10	AEC Q100-012	Short Circuit Characterization	-	10	-		N/A
SER	E11	JESD89-1 JESD89-2 JESD89-3	Soft Error Rate	-	3	-		N/A
LF	E12	AEC-Q005	Lead (Pb) Free: (see AEC-Q005)	-	-	-	Done	Generic Data applied (see INN3977CQ)

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
TEST GROUP F – DEFECT SCREENING TESTS								
PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	All	All	All	Reject units outside Avg.	Done
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)	All	All	All	Reject units outside criteria	Done
TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS (for Ceramic Package testing only)								
MS	G1	JESD22 B104	Mechanical Shock: (Test @ Rm)	-	15	-	of	N/A
VFV	G2	JESD22 B103	Variable Frequency Vibration: (Test @ Rm)	-	15	-	of	N/A
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration: (Test @ Rm)	-	15	-	of	N/A
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak:	-	15	-	of	N/A
DROP	G5	----------	Drop Test: (Test @ Rm) MEMS cavity parts only. Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.	-	5	-	of	N/A
LT	G6	MIL-STD-883 Method 2004	Lid Torque:	-	5	-	of	N/A
DS	G7	MIL-STD-883 Method 2019	Die Shear:	-	5	-	of	N/A
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor:	-	3	-	of	N/A