Title	***Reference Design Report for 60 W Power Supply with 5 V – 20 V Output Using InnoSwitch™4-Pro PowiGaN™ INN4373F-H341, ClampZero™ CPZ1075M and Microchip's PIC16F18325 Microcontroller***
Specification	90 VAC – 265 VAC Input; 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 3 A;
Application	Programmable Industrial Power Supply
Author	Applications Engineering Department
Document Number	RDR-961
Date	January 18, 2023
Revision	1.0

Summary and Features

- InnoSwitch4-Pro: Digitally Controllable Off-line CV/CC ZVS Flyback Integrated Switcher IC with 750 V PowiGaN, Active Clamp Drive and Synchronous Rectification
  - Comprehensive protection features with telemetry for power supply status and fault monitoring
- Meets DOE6 and CoC v5 2016 Average Efficiency requirements with at least 3.5% pass margin
  - 5 V Output: 92.27% at 115 VAC (10.47% margin); 91.06% at 230 VAC (9.26% margin)
  - 9 V Output: 92.66% at 115 VAC (5.36% margin); 92.72% at 230 VAC (5.42% margin)
  - 15 V Output: 92.70% at 115 VAC (3.80% margin); 93.48% at 230 VAC (4.58% margin)
  - 20 V Output: 92.51% at 115 VAC (3.51% margin); 93.68% at 230 VAC (4.68% margin)
- Meets CoC v5 2016 10% load efficiency requirements with high margin (>10%) for all output voltage conditions
- <15 mW no-load input power at 230 VAC
- Meets CISPR22 / EN55022 Class B conducted EMI with high margin
  - >4.3dB margin at worst case condition (20 V / 3 A, 230 VAC)
- High power density: 10.73 W / inch^3 without enclosure (3.35" x 2.0" x 0.83" form factor)
- Low electrical component count: 72 total

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a power supply using InnoSwitch4-Pro INN4373F-H341. The source capabilities of the power supply are listed below.

- 5 V / 3 A
- 9 V / 3 A
- 15 V / 3 A
- 20 V / 3 A

This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch4-Pro controller providing exceptional performance.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, transformer documentation, and performance data.

Figure 1 – Populated Circuit Board Photograph - Top.

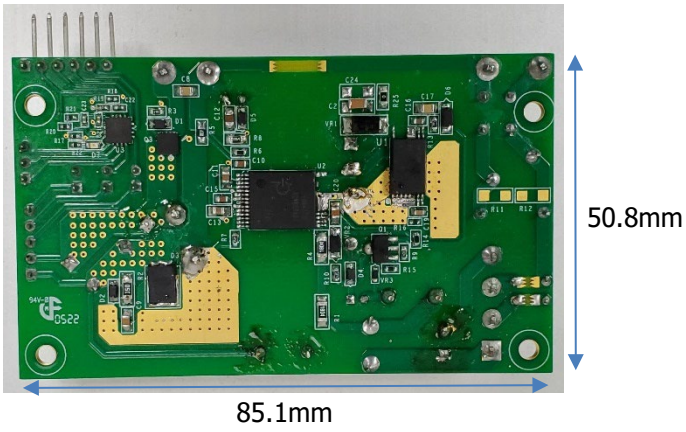


Figure 2 – Populated Circuit Board Photograph - Bottom.

Figure 3 – Populated Circuit Board Photograph (Side View).

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				15	mW	Measured at 230 VAC.
5 V Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			110	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(5\ V)}$			3.0	A	±3%
Average Efficiency	η_{5V}		91.5		%	Measured at 115 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(5\ V)}$			15	W	
9 V Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			110	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(9\ V)}$			3.0	A	±3%
Average Efficiency	η_{9V}		92.0		%	Measured at 115 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(9\ V)}$			27	W	
15 V Setting						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			100	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(15\ V)}$			3.0	A	±3%
Average Efficiency	η_{15V}		92.0		%	Measured at 115 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(15\ V)}$			45	W	
20 V Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			100	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(20\ V)}$			3.0	A	±3%
Average Efficiency	η_{20V}		92.5		%	Measured at 115 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(20\ V)}$			60	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

Note A: Output Voltage Ripple is measured at the end of 100mΩ cable with the probe having decoupling capacitors 47 μF electrolytic and 100 nF ceramic in parallel.

B: Output Current Limit Accuracy is within ±150 mA for Operating Current between 1 A and 3 A, or ±5% for Operating Current >3 A.

Note: Output terminals in this design don't support a Type-C connector. To use this design for a charger/adapter with a different shape and form factor, the changes in the circuit board layout must be carefully evaluated to meet the target specifications for EMI, ESD, and Line Surge performance.

3 Schematic

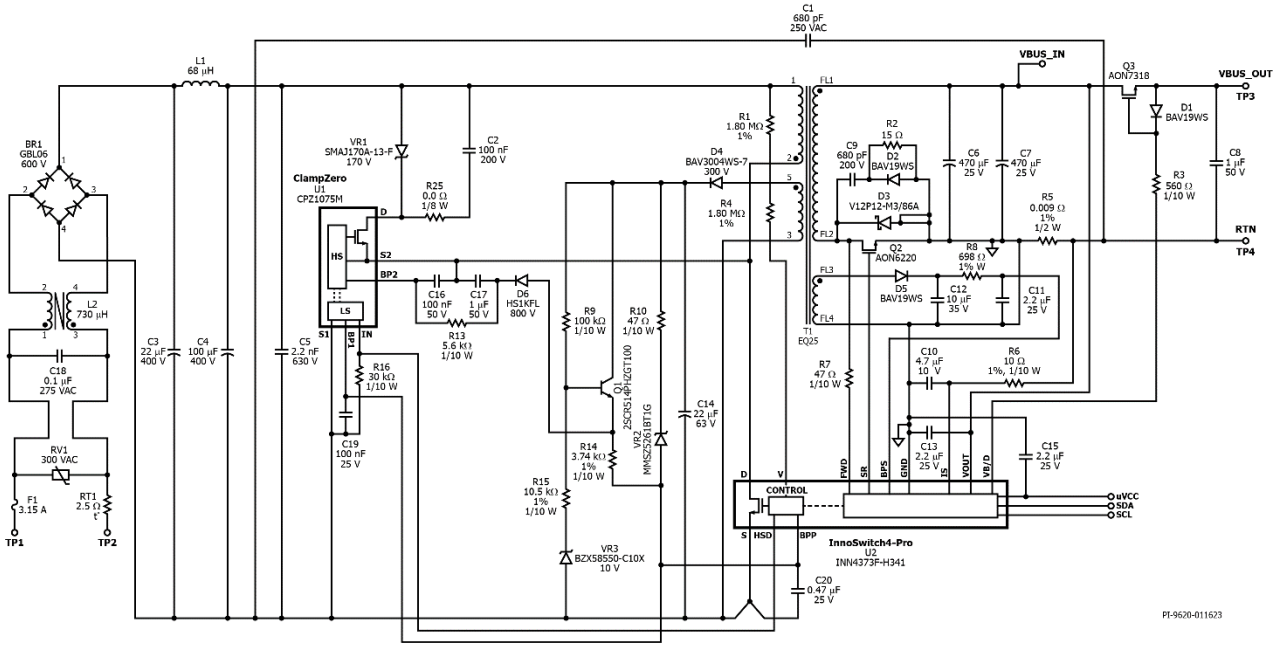


Figure 4a – Power Circuit Schematic, PI-9620-110822

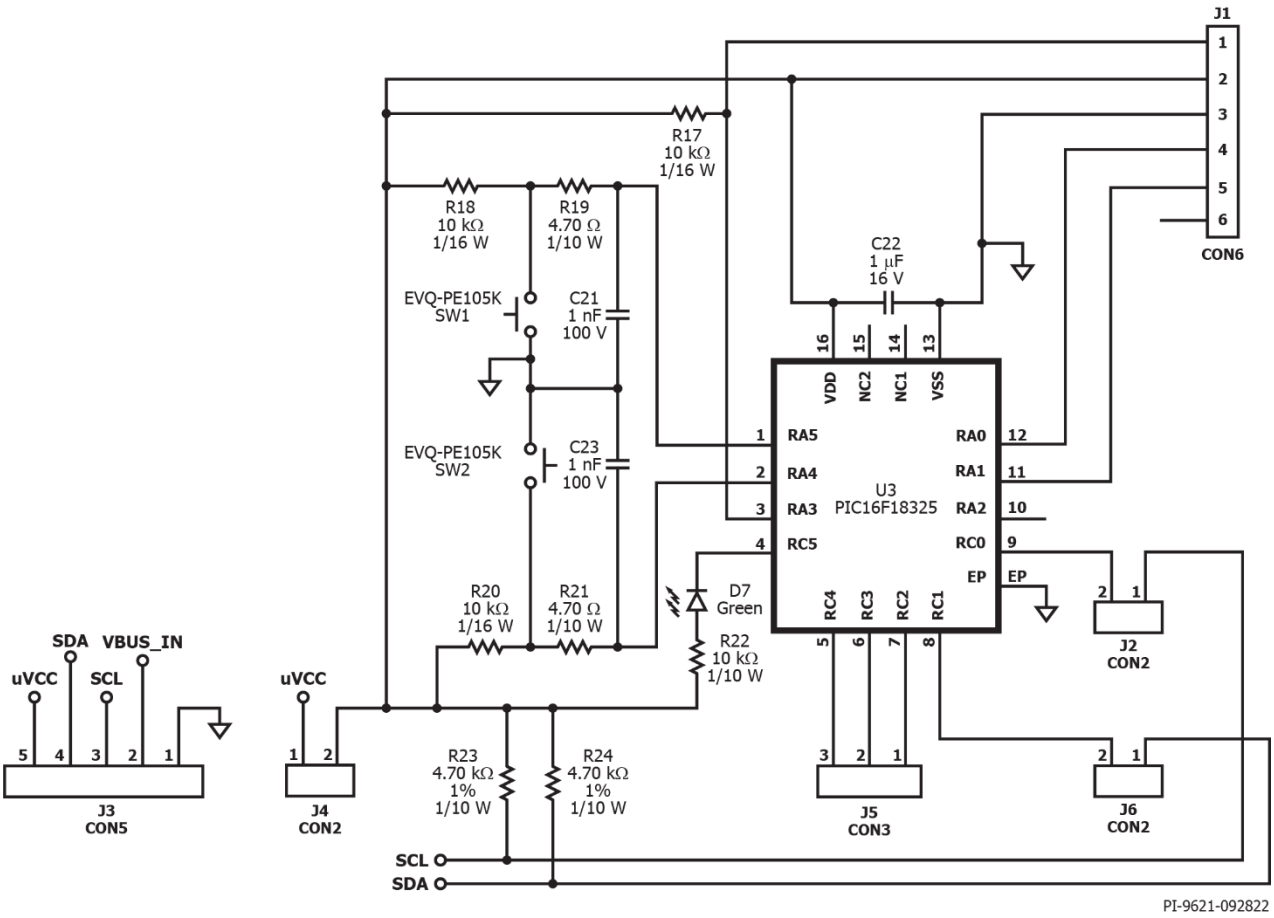


Figure 4b – Microcontroller Circuit Schematic, PI-9621-092822

4 Circuit Description

4.1 Input Rectifier and EMI Filter

The input fuse F1 isolates the circuit and provides protection from component failure. Metal oxide varistor RV1 offers protection during line surge events by effectively clamping the input voltage seen by the power supply. Inrush thermistor RT1 limits the inrush current when the power supply is connected to the AC input. Common mode choke L2 along with Y-capacitor C1 provides common mode noise filtering while inductor L1 forms a pi filter with capacitors C3 and C4 for differential mode EMI filtering along with the X-capacitor C18. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitors C3 and C4.

4.2 InnoSwitch4-Pro IC Primary

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch4-Pro IC (U2). Resistors R1 and R4 provide input voltage sensing for protection in case of AC input under voltage or overvoltage.
The primary clamp formed by the body diode of the ClampZero IC and capacitor C2 limit the peak drain voltage of U2 at the instant of turn-off of the switch inside U2. The energy stored in the leakage inductance of the transformer will be transferred to capacitor C2. Part of the magnetizing energy will also get transferred to C2 depending on the capacitance value used. VR1 is used to protect the InnoSwitch4-Pro from excessive drain voltages during abnormal conditions applied to the power supply. High voltage ceramic capacitor C5 is used to decouple the bulk voltage, reducing the loop area of high frequency switching currents.

When the FluxLink signal is received from the secondary-side, the InnoSwitch4-Pro IC generates an HSD (High Side Drive) signal to turn on the ClampZero device. When the ClampZero IC (U1) turns on, to achieve soft switching of the InnoSwitch4-Pro primary switch, clamp capacitor C2 starts to charge the leakage inductance of the transformer in the case of CCM operation and both the leakage and the magnetizing inductance of the transformer in the case of DCM operation. A small delay is provided from the instant the high-side switch turns off to achieve zero voltage switching on the primary switch. This delay is either programmable by resistor R16 value at low-line input voltage, or a fixed 500 ns delay at high-line input voltage. The transition between programmable delay and fixed delay is based on input line voltage information at the V pin of InnoSwitch4-Pro IC.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C20 when AC is first applied. During normal operation, the primary side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D4 and filtered using capacitor C14. Linear regulator circuit comprises of BJT Q1, R9, R15, and Zener diode VR3 ensures sufficient current flows through R14 into the BPP pin of the InnoSwitch4-Pro and the BP1 pin of the ClampZero

ICs. By injecting sufficient current into BPP and BP1 pins, the internal current source of U2 is not required to charge C20, and power consumption is minimized during no-load condition and at normal operation.

Capacitor C19 is used to provide local decoupling at the BP1 pin of IC U1. Capacitor C16 provides the decoupling for BP2 pin. Diode D6 and capacitor C17 form a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R13 limits the current flowing into the BP2 pin.

Zener diode VR2 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2 which then causes excess current to flow into the BPP pin of InnoSwitch4-Pro IC. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch4-Pro controller will latch off and prevent any further increase in output voltage. Resistor R10 limits the current injected to BPP pin when the output overvoltage protection is triggered.

4.3 InnoSwitch4-Pro IC Secondary

The secondary-side of the InnoSwitch4-Pro IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side synchronous rectifier FET (SR FET) Q2 and filtered by capacitors C6 and C7. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via an RCD snubber, R2, C9, and D2. Diode D2 minimizes the dissipation in resistor R2. Schottky diode D3 minimizes the losses that happen during the ClampZero switch conduction period.

The gate of Q2 is turned on by secondary-side controller inside IC U2, based on the secondary winding voltage sensed via resistor R7 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding through FluxLink a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. For this design, a secondary bias winding circuit is used to further improve the system efficiency. Bias winding voltage is rectified by diode D5 and filtered by capacitor C12. Resistor R8 limits the current flowing to the BPS pin of U2. Capacitor C11 connected to the BPS pin of InnoSwitch4-Pro IC provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R5. The current measurement is filtered with resistor R6 and capacitor C10, and then monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of up to approximately 32 mV configured by the microcontroller via I^2C interface is used to reduce the losses. Once the threshold is exceeded, the InnoSwitch4-Pro IC responds depending on its configuration to either maintain a fixed output current by using variable frequency and variable primary switch peak current limit control schemes to maintain a fixed output current or to shut down the power supply.

For constant current (CC) operation, when the output voltage falls below 5 V, the secondary-side controller inside InnoSwitch4-Pro IC will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C11 via resistor R7 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level, the unit enters auto-restart until the output load is reduced.

When output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch4-Pro IC. Similar to current regulation, the output voltage is also compared to an internal voltage threshold that is set via the integrated secondary controller of the InnoSwitch4-Pro IC and Microcontroller IC, and output voltage regulation is achieved by variable frequency and variable primary switch peak current limit control schemes. Capacitor C13 is used as decoupling capacitor for the VOUT pin.

N-channel MOSFET Q3 functions as the bus switch which connects or disconnects the output of the flyback converter to the power supply output. MOSFET Q3 is controlled by the VB/D pin on the InnoSwitch4-Pro IC. Diode D1 is connected across the Source and Gate terminals of Q3 and resistor R3 is connected from the Gate terminal of Q3 to the VB/D pin to provide a discharge path for the bus voltage when Q3 is turned off. Capacitor C8 is used at the output for ESD protection and output voltage ripple reduction.’

4.4 Microcontroller

This design uses PIC16F18325-I/JQ microcontroller. This device is powered directly from the uVCC pin of InnoSwitch4-Pro (U2). Communication between these 2 devices occur through I^2C interface through the I^2C interface using the SCL and SDA lines in which it sets several command registers, such as the CV, CC, VKP, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output under voltage threshold registers of the InnoSwitch4-Pro IC, respectively. The status of the InnoSwitch4-Pro IC is read by the Microcontroller from the telemetry registers also using the I^2C interface.

Capacitor C15 is used as decoupling capacitor on uVCC pin of U2. Resistors R23 and R24 are used as pull-up resistors for SCL and SDA respectively.

Capacitor C22 is used as decoupling capacitor on VDD pin of U3. Resistors R18, R19, R20, R21, Capacitors C21, C23 along with Switches SW1 and SW2 are used increment/decrement CV, CC, VKP parameters based on different configurations of J5 (CON3)f connector. Step by step process to change these parameters will be described in the following sections of this document.

4.5 Digitally Controlled Feature

In this design, PIC16F18325 is the I^2C Master and InnoSwitch4-Pro is the Slave device. The output of the InnoSwitch4-Pro powers the MCU directly to its µVCC output pin.

The PIC microcontroller communicates over its I^2C lines to the SDA and SCL pins (which are both 3.3 V and 5 V compatible) of the InnoSwitch4-Pro IC. The SDA and SCL lines need pull-up resistors R24 and R23 respectively to the µVCC pin. The µVCC pin needs a decoupling capacitor C15.

The MCU enables dynamic control of output voltage and current along with many configurable features through I^2C communication. I^2C Communication is set to 400 kHz on this design.

4.6 Debounce Switches

Two debounce switches are present on the board. When Idle, the switches are pulled high (+3.3 V). When pressed, they are grounded. On each button press I^2C commands are generated to perform the following changes based on the configuration of J5 (CON3) connector as described below.

Figure 5 – Pin Configuration for J5 (CON3).

Configuration 1: Pins 1, 2 and 3 open (Not connected to any point)

Identification: Green LED always ON
Function: CV value change, Turn ON/OFF Bus switch

Switch 1 (SW1) Functions:

Action	Function
Single Click	1 V Increment
Double Click	100 mV Increment
Long press (~5sec)	Bus switch OFF

Switch 2 (SW2) Functions:

Action	Function
Single Click	1 V Decrement
Double Click	100 mV Decrement
Long press (~2sec)	Bus switch ON

CV value change

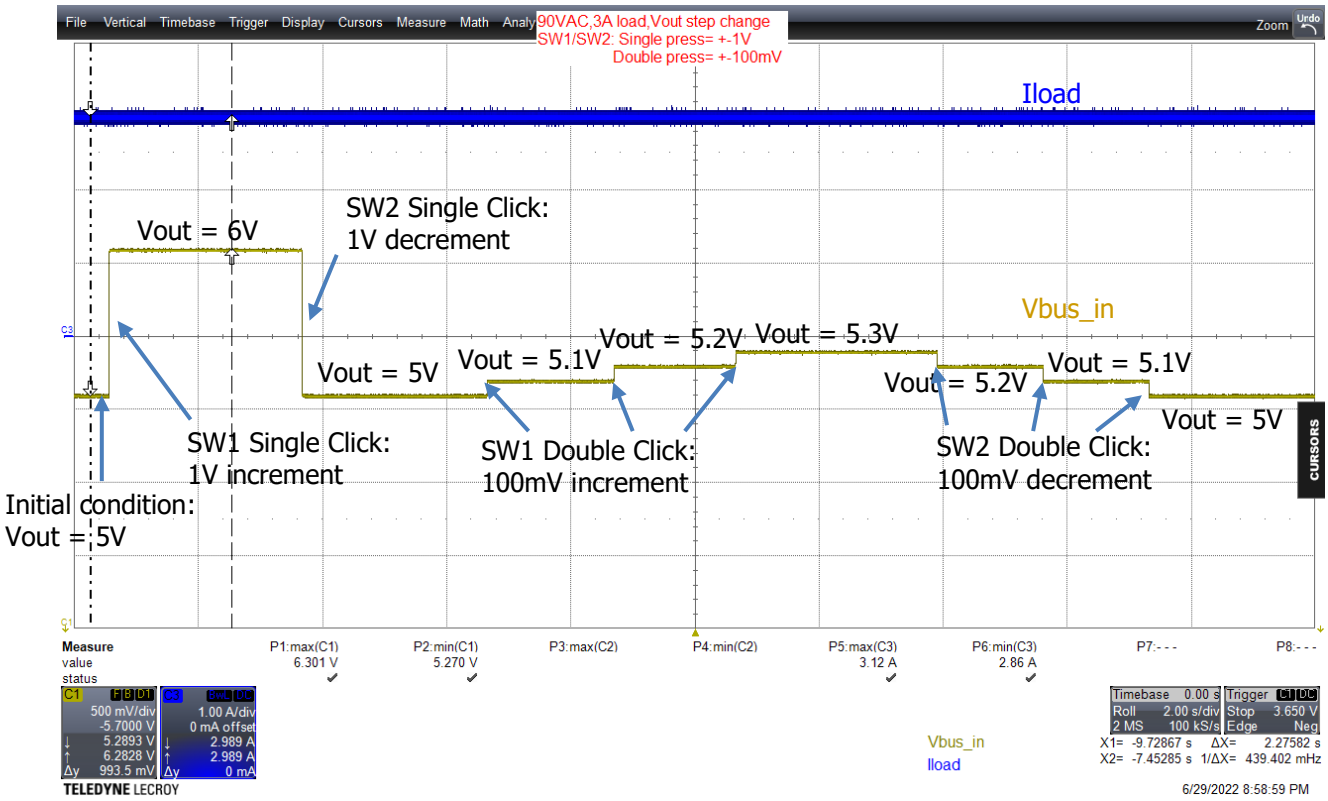


Figure 6a – Waveform Representing Vout Change.

Bus Switch ON/OFF

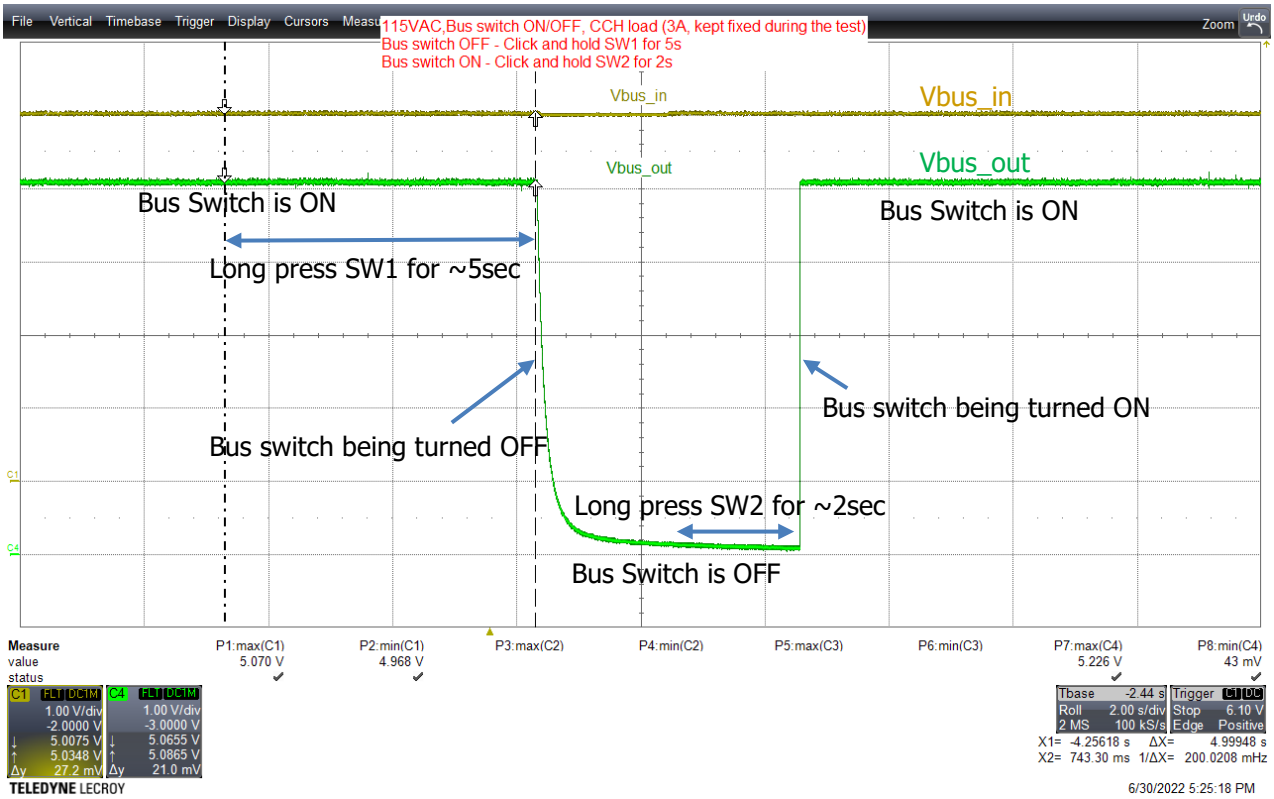


Figure 6b – Waveform Representing Bus Switch ON/OFF.

Configuration 2: Pins 1 and 2 shorted with a jumper

Identification: Green LED blinks fast (every 300ms)
Function: CC limit change

Switch 1 (SW1) Functions:

Action	Function
Single Click	5 LSB increment
Double Click	1 LSB increment

Switch 2 (SW2) Functions:

Action	Function
Single Click	5 LSB decrement
Double Click	1 LSB decrement

CC limit change

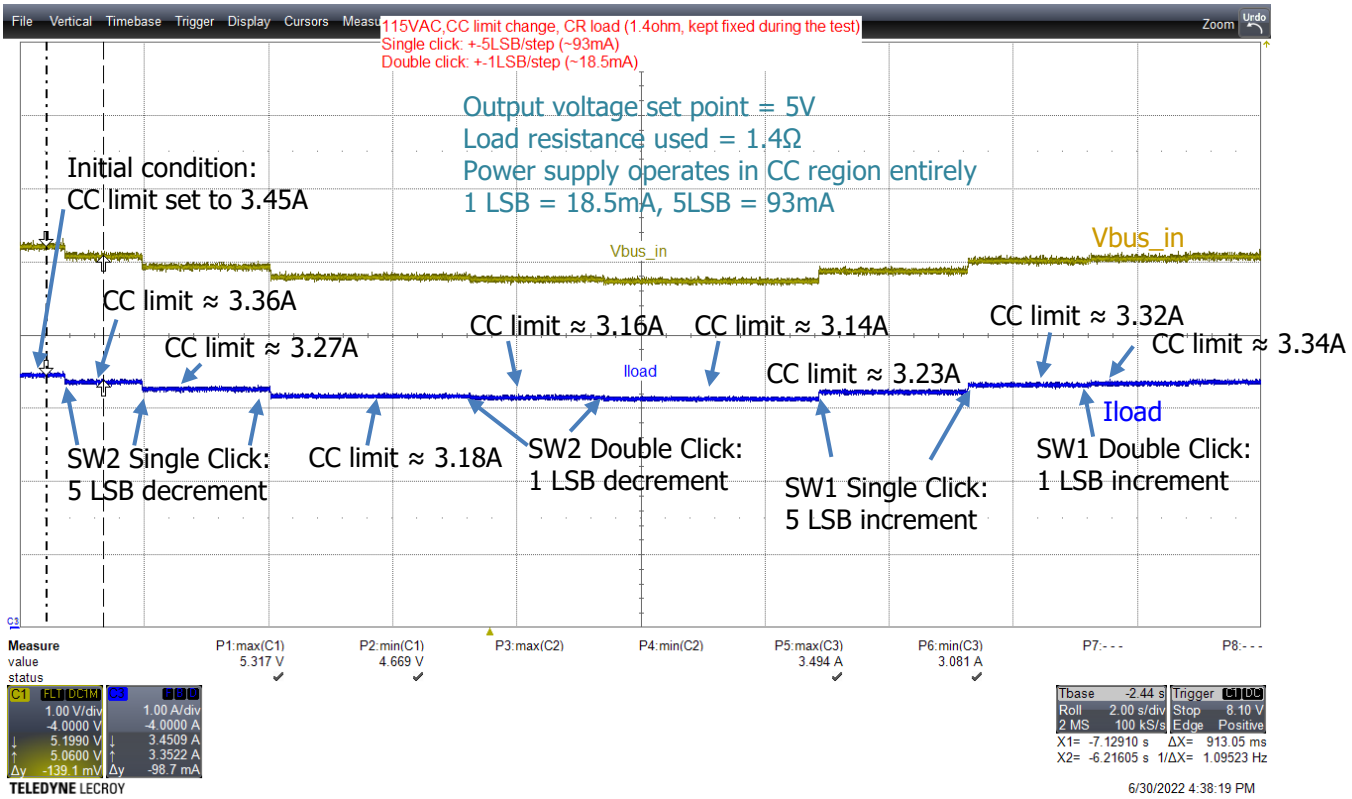


Figure 6c – Waveform Representing CC Limit Change.

Configuration 3: Pins 2 and 3 shorted with a jumper

Identification: Green LED blinks slow (every 1s)
Function: VKP value change

Switch 1 (SW1) Functions:

Action	Function
Single Click	1 V Increment
Double Click	100 mV Increment

Switch 2 (SW2) Functions:

Action	Function
Single Click	1 V Decrement
Double Click	100 mV Decrement

VKP value change

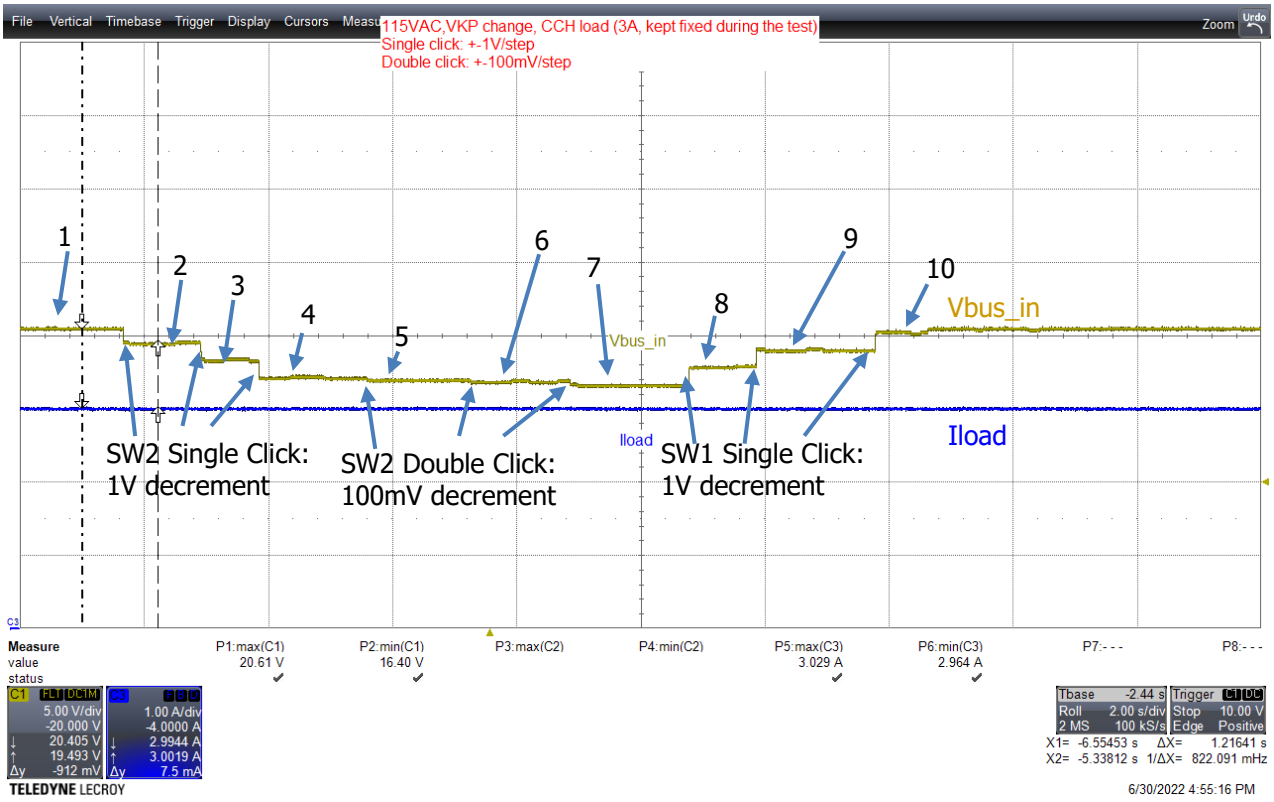


Figure 6d – Waveform Representing VKP Value Change.

1) Initial condition: VKP value set to 20 V
2) VKP value decreased to 19 V
3) VKP value decreased to 18 V
4) VKP value decreased to 17 V
5) VKP value decreased to 16.9 V
6) VKP value decreased to 16.8 V
7) VKP value decreased to 16.7 V
8) VKP value increased to 17.7 V
9) VKP value increased to 18.7 V
10) VKP value increased to 19.7 V

5 PCB Layout

PCB copper thickness is 0.062 inches.

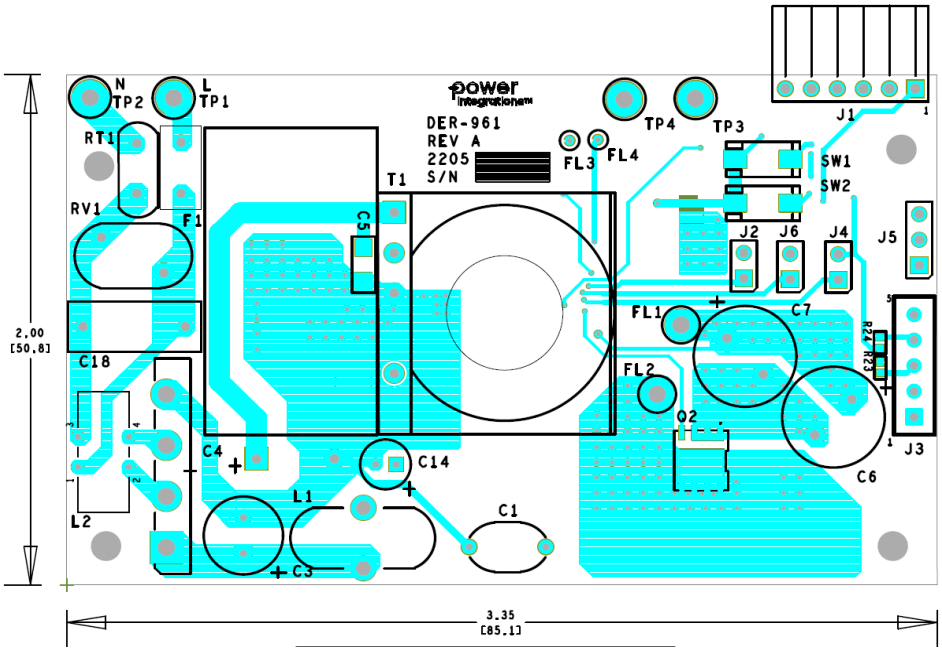


Figure 7 – Printed Circuit Layout, Top.

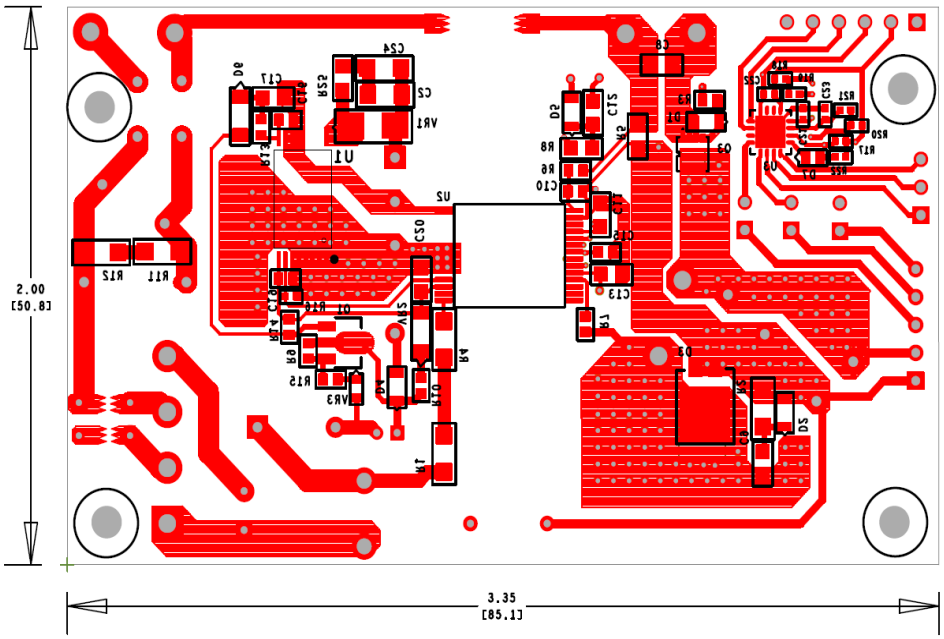


Figure 8 – Printed Circuit Layout, Bottom.

Note: Component references R11, R12 and C24, although present in the layout, should not be populated.

6 Bill of Materials

6.1 Electrical parts

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	DIODE BRIDGE 600V 4A GB	GBL06	Genesic Semi
2	1	C1	680pF, ±10%, 250VAC, X1, Y1, Ceramic, B, Radial, Disc	DE1B3RA681KN4AN01F	Murata Electronics
3	2	C2	100 nF, 200 V, Ceramic, X7R, 1206	C1206C104K2RACTU	Kemet
4	1	C3	22 uF, 400 V, Electrolytic, 8 x 16	ERK2G9220F16OTO	Aishi
5	1	C4	100 uF, 400 V, Electrolytic, Low ESR, (16 x 30)	EPAG401ELL101ML30S	Nippon Chemi-Con
6	1	C5	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K115AA	TDK
7	2	C6 C7	470 uF, 25 V, ±20%, Al Organic Polymer, Gen. Purpose, Can, 15 mOhm, 2000 Hrs @ 105°C	A750MS477M1EAAE015	KEMET
8	2	C8 C17	1 uF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
9	1	C9	680 pF 200V X7R MULTI-LAYER CERAMIC +/- 10 %	C0805C681K2RACAUTO	Kemet
10	1	C10	4.7 uF, ±10%, 10V, Ceramic, X7S, 0603, -55°C ~ 125°C, Low ESL	C1608X7S1A475K080AC	TDK
11	2	C11 C13	2.2 µF, ±10%, 25V, Ceramic X7R, 0805	CL21B225KAFNFNE	Samsung
12	1	C12	10 µF ±10%, 35V Ceramic X5R 0805	C2012X5R1V106K125AC	TDK
13	1	C14	22 uF, ±20%, 63 V, Electrolytic, (5 x 12.5), LS 2 mm	63YXJ22M5X11	Rubycon
14	1	C15	2.2 uF,±10%, 25 V, Ceramic, X7R, 0603,-55 to 125 °C	GRM188Z71E225KE43D	Murata
15	1	C16	0.1 µF, ±10% 50V Ceramic X7R 0603	CGA3E2X7R1H104K080AA	TDK
16	1	C18	0.1µF, 20%, 275VAC, 560VDC, X2, -40°C ~ 110°C, 5 mm W x 13 mm L x 11.1 mm H	R46KF310000P1M	KEMET
17	1	C19	100 nF, 0.1µF, ±10%, 25V, Ceramic, X7R, General Purpose, -55°C ~ 125°C, 0603	CL10B104KA8NFNC	Samsung
18	1	C20	0.47 uF, ±10%,25 V, Ceramic, X7R, 0805	CGA4J2X7R1E474K125AA	TDK
19	2	C21 C23	1 nF 100 V, Ceramic, X7R, 0402	GCM155R72A102KA37D	Murata
20	1	C22	1 uF, ±10%, 16V, X5R, 0402	CL05A105KO5NNNC	Samsung
21	3	D1 D2 D5	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
22	1	D3	Diode, Schottky, 120V, 12A, Surface Mount, TO-277A (SMPC)	V12P12-M3/86A	Vishay
23	1	D4	DIODE, GEN PURP, FAST RECOVERY, 300V, 225mA, SOD323	BAV3004WS-7	Diodes, Inc.
24	1	D6	800V, 1 A, High Efficiency Fast Recovery, SOD-123FL	HS1KFL	Taiwan Semi
25	1	D7	LED, GREEN,525nm, 3.2 V, 20 mA, 260.5mcd, RECT, CLEAR, 0603	LTST-C194TGKT	Lite-On Inc
26	1	F1	3.15 A, 250V, Slow, RST	RST 3.15-BULK	Belfuse
27	1	L1	68 µH, Unshielded Toroidal Inductor, 2A, 55mOhm Max, Radial, Vertical (Open)	7447033	Wurth
28	1	L2	730 uH, Toroidal Common Mode Choke, custom, DER-961, wound on 32-00330-00 core.	32-00440-00	Power Integrations
29	1	Q1	NPN, 80V 0.7A, MEDIUM POWER,TO-243AA, SOT-89	2SCR514PHZGT100	Rohm Semi
30	1	Q2	MOSFET, N-CH, Peak rating 120V for 10us, 48A (Tc), 113.5W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
31	1	Q3	N-Channel 30 V 36.5 A (Ta), 50A (Tc) 4.1 W (Ta), 39 W (Tc) SMT 8-DFN-EP (3.3x3.3), 8DFN, 8-PowerVDFN	AON7318	Alpha & Omega Semi
32	2	R1 R4	RES, 1.80 M, 1%, 1/4 W, Thick Film, 1206	AC1206FR-071M8L	Yageo
33	1	R2	RES, 15 R, 5%, 1/4 W, Thick Film, 1206	ERJ-P08J150V	Panasonic
34	1	R3	RES, 560 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ561V	Panasonic
35	1	R5	RES, 0.009 R, ±1%, 0.5 W, 0805, Current Sense, Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns
36	1	R6	RES, 10 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
37	2	R7 R10	RES, 47 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
38	1	R8	RES, 698 R, 1%, 1/4 W, Thick Film, 1206	CR1206-FX-6980ELF	Bourns Inc.
39	1	R9	RES, 100 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
40	1	R13	RES, 5.6 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ562V	Panasonic
41	1	R14	RES, 3.74 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3741V	Panasonic

42	1	R15	RES, 10.5 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1052V	Panasonic
43	1	R16	RES, 30 k, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ303X	Panasonic
44	4	R17 R18 R20 R22	RES, 10 K, 5%, 1/16 W, Thick Film, 0402	RC0402JR-0710KL	Yageo
45	2	R19 R21	RES, 470, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ471X	Panasonic
46	2	R23 R24	RES, 4.70 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF4701X	Panasonic
47	1	R25	RES, 0 R, 5%, 1/8 W, Thick Film, 0805	RMCF0805ZT0R00	Stackpole
48	1	RT1	NTC Thermistor, 2.5 Ohms, 3 A	SL08 2R503	Ametherm
49	1	RV1	300 Vac, 25 J, 7 mm, RADIAL	V300LA4P	Littlefuse
50	2	SW1 SW2	SWITCH TACTILE SPST-NO 0.05A 12V	EVQ-PE105K	Panasonic
51	1	T1	Custom, DER-961 Transformer EQ25, Lp=640uH		Power Integrations
52	1	U1	ClampZero, CPZ1075M, MinSOP-16	CPZ1075M	Power Integrations
53	1	U2	InnoSwitch4-Pro, InSOP-T28D	INN4373F-H341	Power Integrations
54	1	U3	IC, PIC, PIC®, XLP™, 16F Microcontroller IC, 8-Bit, 32MHz, 14KB (8K x 14,) FLASH 16-UQFN (4x4)	PIC16F18325-I/JQ	Microchip
55	1	VR1	TVS DIODE, 275V Clamp, 1.4A Ipp, Tvs Diode, Surface Mount, SMA SMAJ (DO-214AC)	SMAJ170A-13-F	Diodes, Inc.
56	1	VR2	DIODE ZENER 47V 500MW SOD123	MMSZ5261BT1G	ON Semi
57	1	VR3	Zener Diode 10 V 300 mW ±5% Surface Mount SOD-523	BZX58550-C10X	Nexperia

Note: Although there is a provision for R11, R12, and C24 in the layout, these parts are not needed and hence not assembled.

6.2 Mechanical Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	TP1	TEST Point, WHT, THRU-HOLE MOUNT	5012	Keystone Electronics
2	2	TP2, TP4	TEST Point, BLK, THRU-HOLE MOUNT	5011	Keystone Electronics
3	1	TP3	TEST Point, RED, THRU-HOLE MOUNT	5010	Keystone Electronics

7 Transformer Specification

7.1 Electrical Diagram

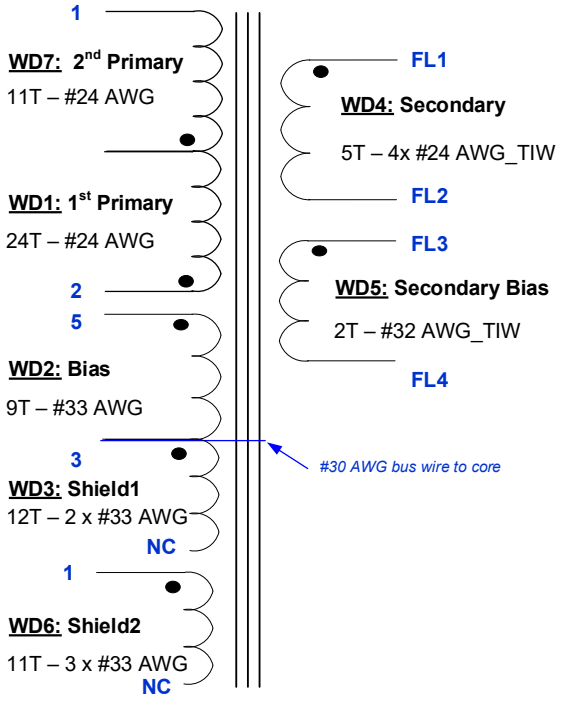


Figure 9 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	60 secs, 60 Hz, from Pins 1- 5 to FL1-FL2, 1 mA max	3000Vac
Primary Inductance	Pins 1-2, all other open, measured at 100kHz, 1.0V test level	640 uH, +/-5%
Resonant Frequency	Pins 1-2, all other open	1000 kHz (Min.)
Primary Leakage	Pins 1-2, with 7-10 shorted, measured a t65KHz, 0.4Vrms	6.5 μH +/- 5%

7.3 Transformer Build Diagram

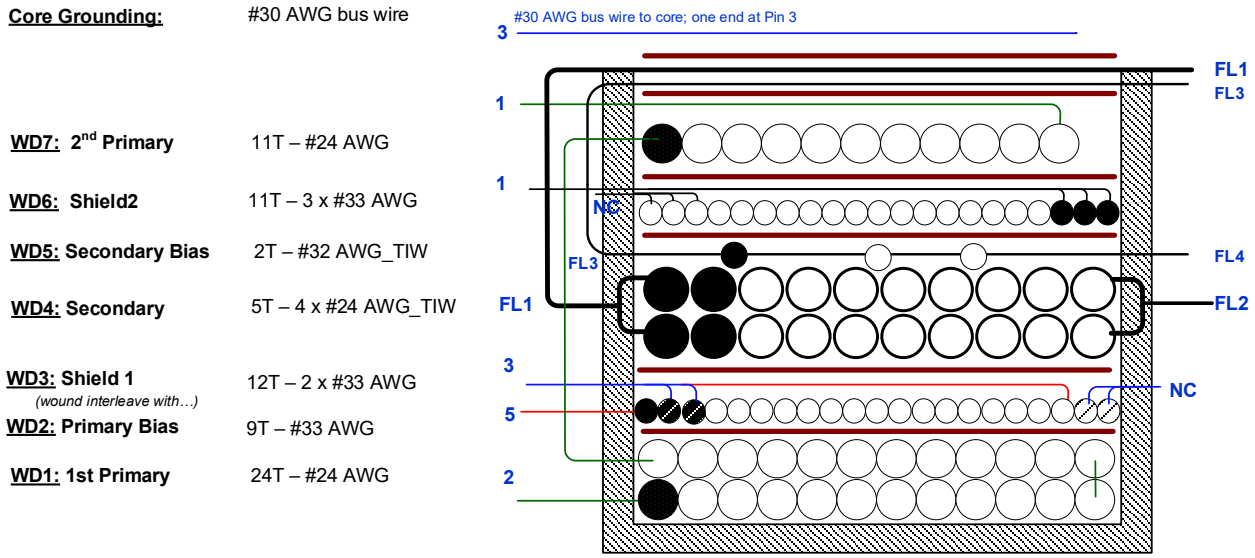


Figure 10 – Transformer Build Diagram.

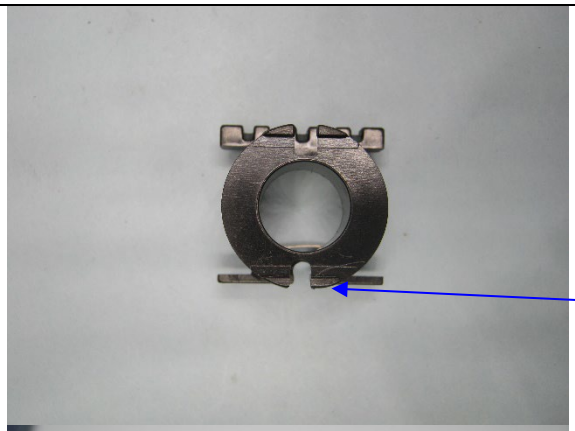
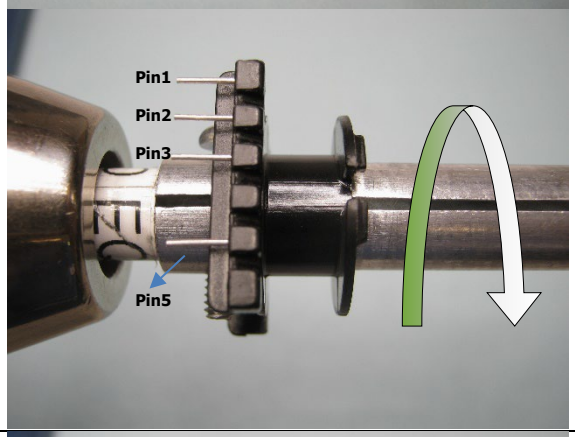
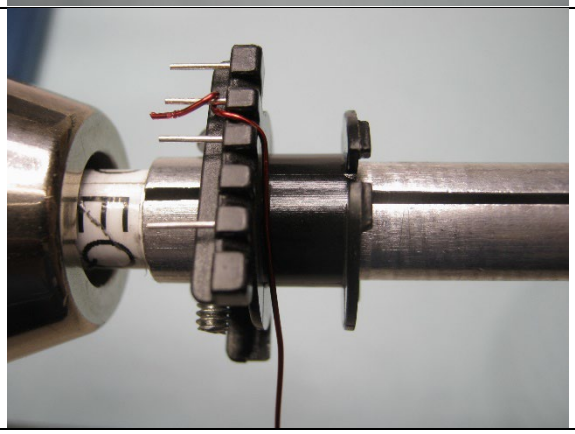
7.4 Material List

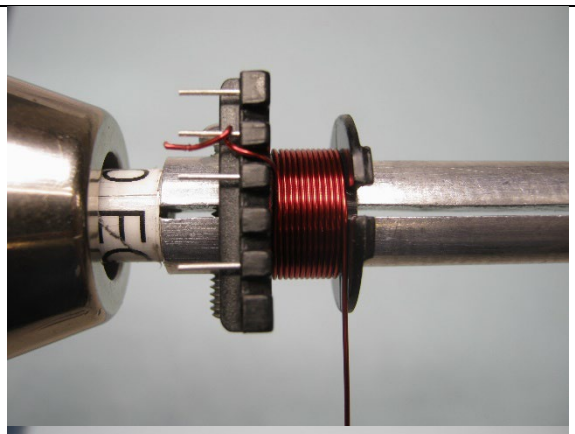
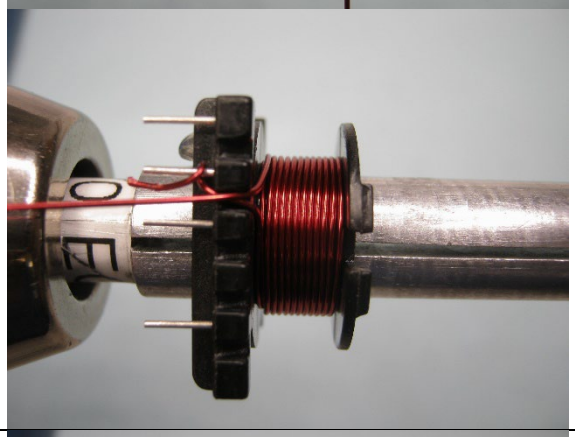
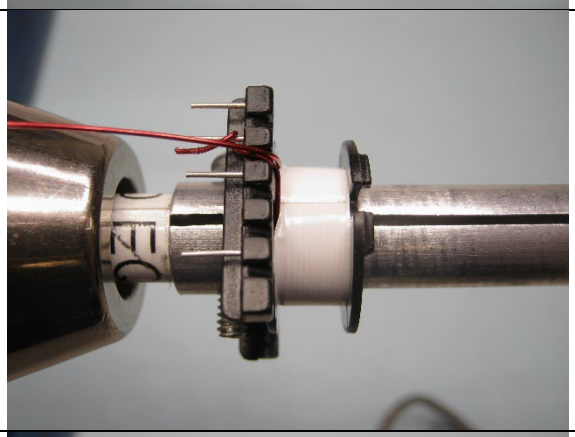
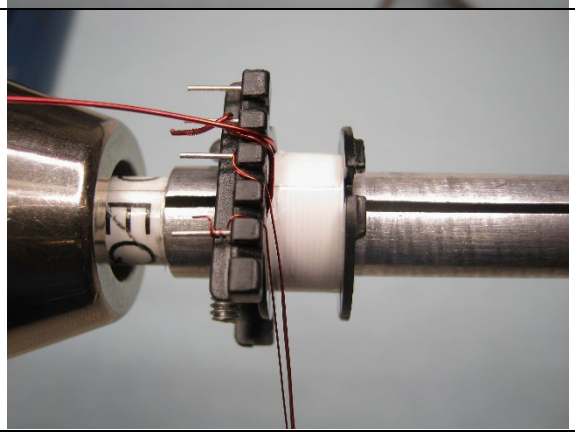
Item	Description
[1]	Core: EQ25, Material 3C95. FerroxCube.
[2]	Bobbin. EQ25-V-6pins. PI#: 25-01136-00.
[3]	Magnet Wire: #24 AWG, Double Coated.
[4]	Magnet Wire: #33 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Magnet Wire: #32 AWG, Triple Insulated Wire.
[7]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 8.0 mm Wide.
[8]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 12.0 mm Wide.
[9]	Bus Wire: #30AWG, Alpha Wire, Tinned Copper.
[10]	Glue: Loctite, 409, Gel, Mf #:40904; or equivalent.
[11]	Tape: 3M 1298 Polyester Film, 1 mil thick, 30mm x 56mm.
[12]	Epoxy: Devcon, 5 mins Epoxy, Mfr#: 14270; or equivalent.
[13]	Varnish: Dolph BC-359; or equivalent.

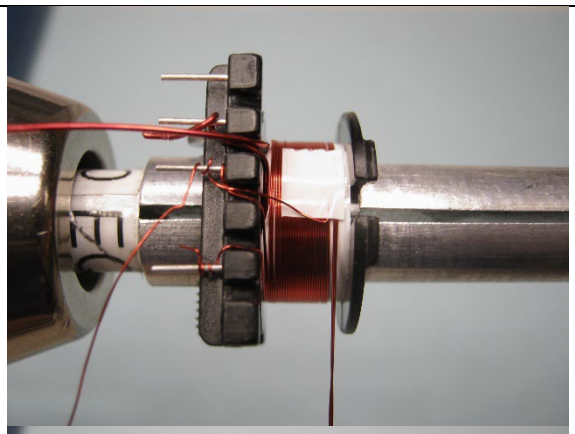
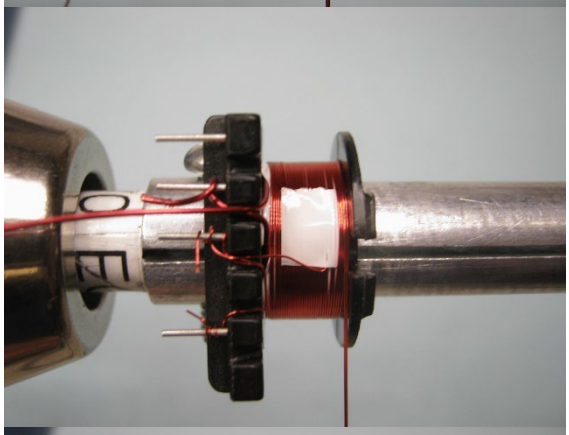
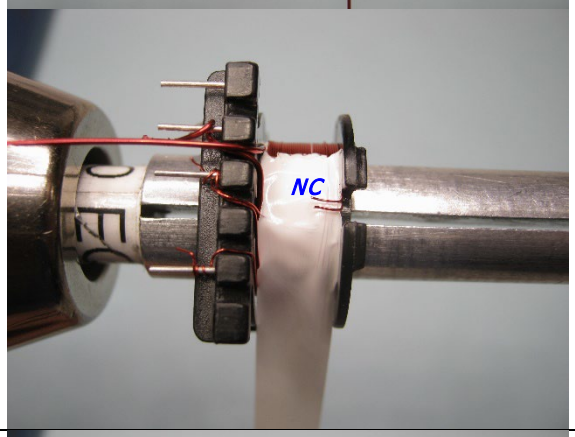
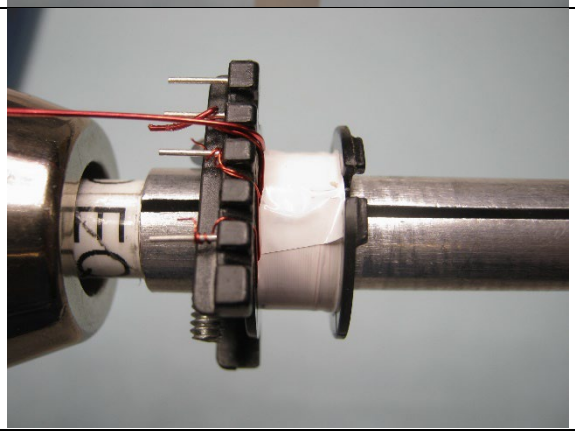
7.5 Transformer Instruction

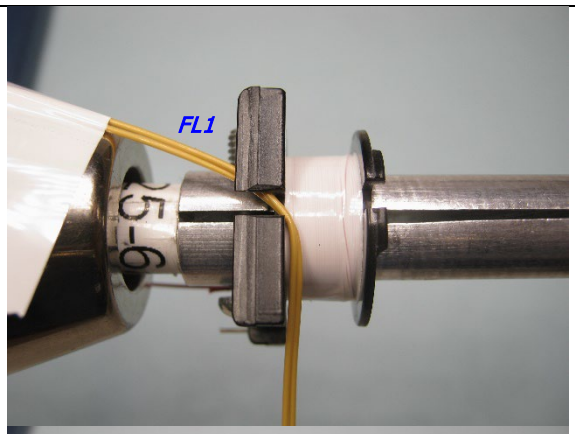
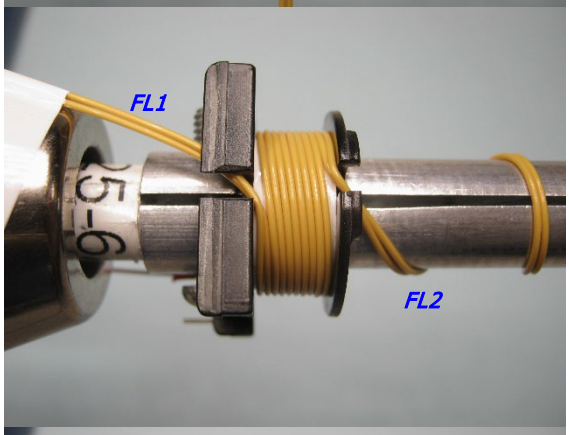
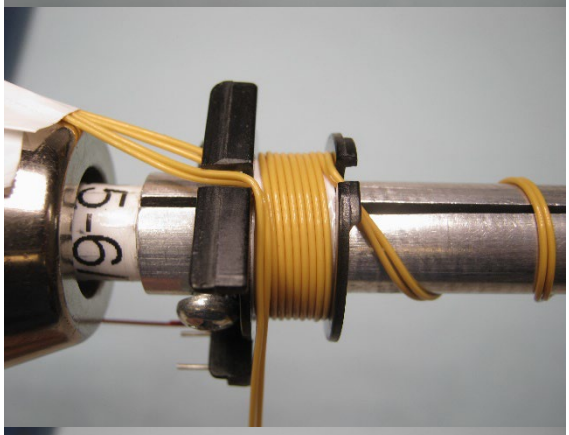
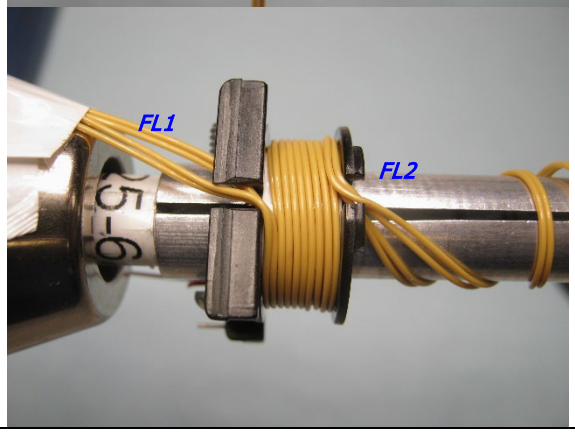
Winding Preparation	Make 3 slots with 3mm wide on bobbin for Secondary wires enter and exit, *(see pictures below).* Position the bobbin item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction.
WD1 1st Primary	Start at pin 2, wind 24 turns of wire item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn exit the wire and leave enough length floating for 2nd Primary winding.
Insulation	1 layer of tape item [7].
WD2: Bias & WD3: Shield1	Use 1 wire item [4] start at pin 5 for Bias winding, also use 2 wires same item [4] start at pin 3 for Shield1 winding. Wind all 3 wires in parallel, at the 9th turn, place a piece of tape to hold the wires, bring 1 wire of Bias winding to the left and terminate at pin 3. Continue winding to 12th turn, cut short 2 wires for Shield1 Winding as No-Connect.
Insulation	1 layer of tape item [7].
WD4 Secondary	Start at left slot of secondary side, use 2 wires item [5], leaving ~ 40.0mm floating, and mark as FL1.Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0mm floating, and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2 respectively.
WD5 Secondary Bias	Also start at left slot of secondary, use 1 wire item [6], wind 2 turns with the same way above, start lead FL3 and end lead FL4.
Insulation	1 layer of tape item [7].
WD6 Shield 2	Use 3 wires item [4], start at right with floating ~ 30mm, wind 11 turns from right to left. At the last turn cut short as No-Connect NC, then bring floating wires back to the left and terminate at pin 1.
Insulation	1 layer of tape item [7].
WD7 2nd Primary	Use floating wire from WD1-1st Primary, wind 11 turns from left to right. At the last turn, bring the wire back to the left and terminate at pin 1.
Insulation	1 layer of tape item [7], bring wires FL1 & FL3 from the left to the right and continue with 2 layers of tape to secure all windings and wires.
Finish	Gap cores to get 640uH. Apply 2 layers of tape item [8] onto core sides, *(see pictures below).* Apply glue item [10] at center legs of cores. Solder pin 3 with bus-wire item [9] then lean along core halves and secure with tape. Apply epoxy item [12] between cores to body on top and bottom of the transformer. *(see pictures below).* Varnish with item [13]. Place 2 layers of tape item [11] at the bottom then wrap up to the body of transformer, and tape around 1layer of tape item [7]. (*See pictures below*).

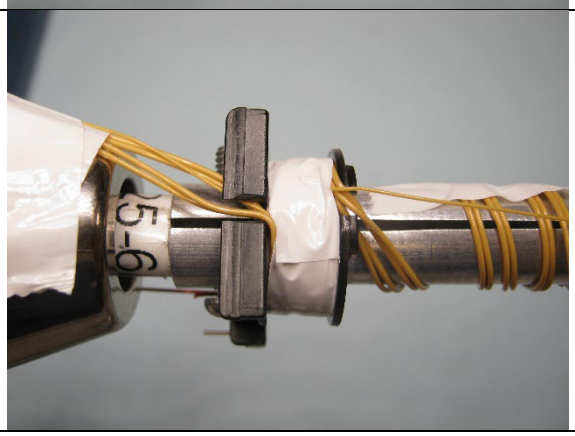
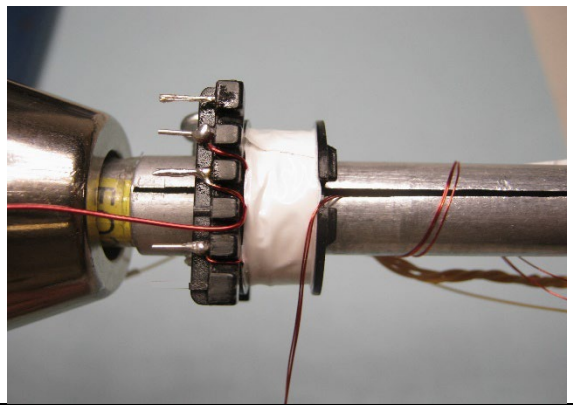
7.6 Transformer Illustrations

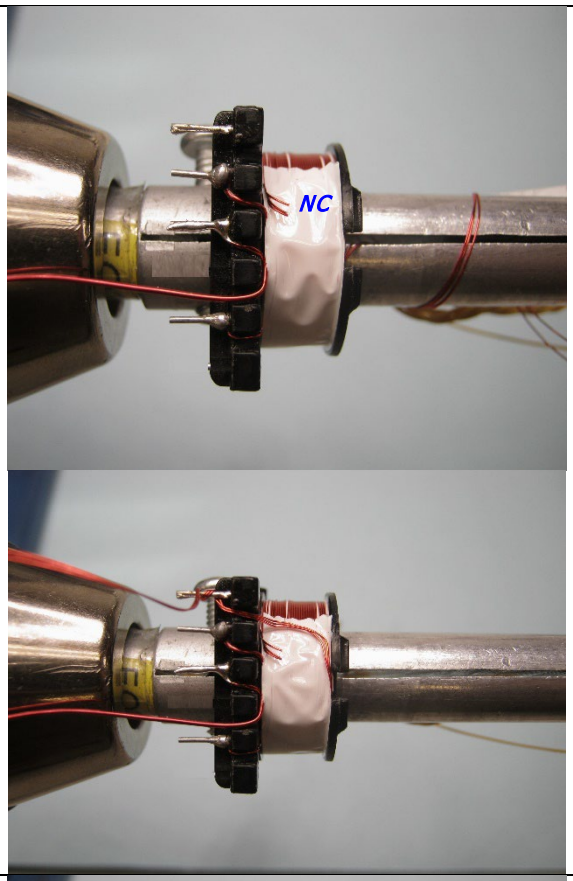
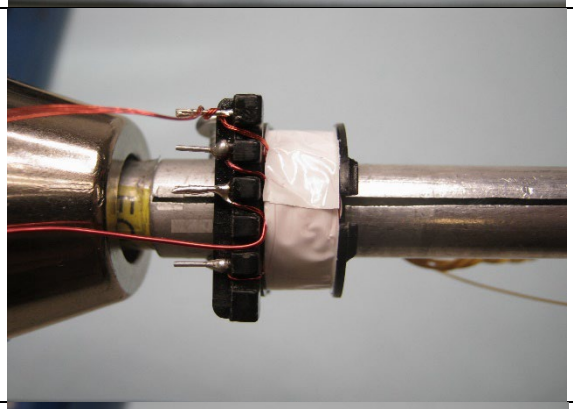
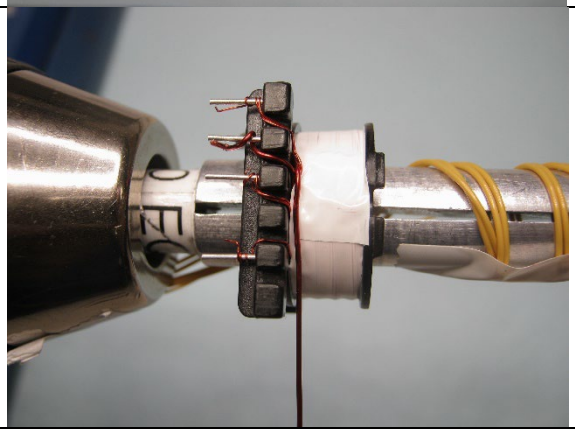
Bobbin Preparation	 	Make 2 slots with 3mm width on bobbin for Secondary wires enter and exit, *(see pictures beside).* Position the bobbin item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction.
WD1 **1st Primary**		Start at pin 2, wind 24 turns of wire item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn exit the wire and leave enough length floating for 2nd Primary winding.

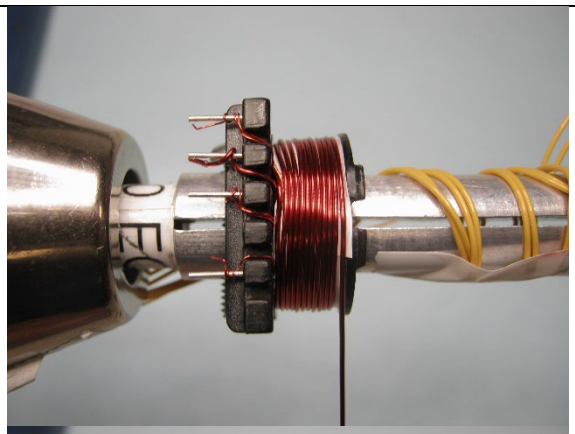
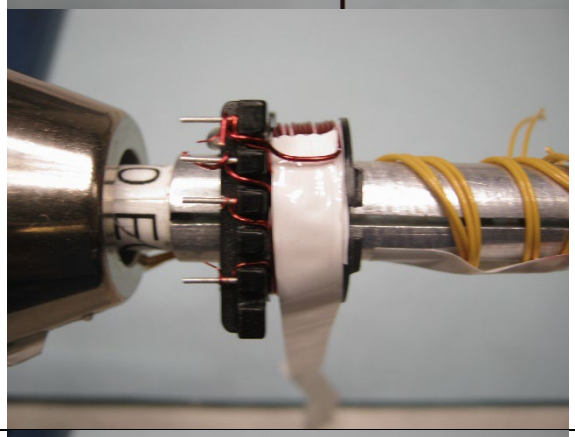
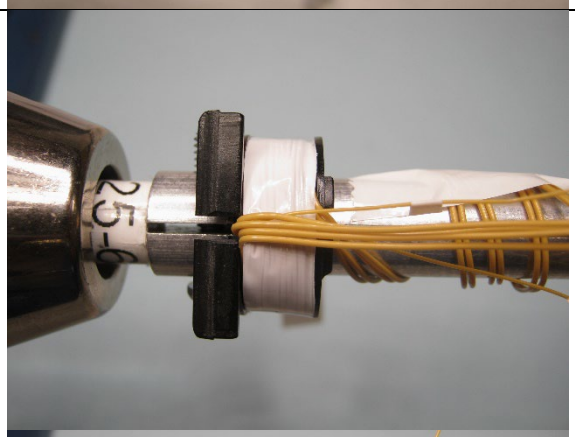
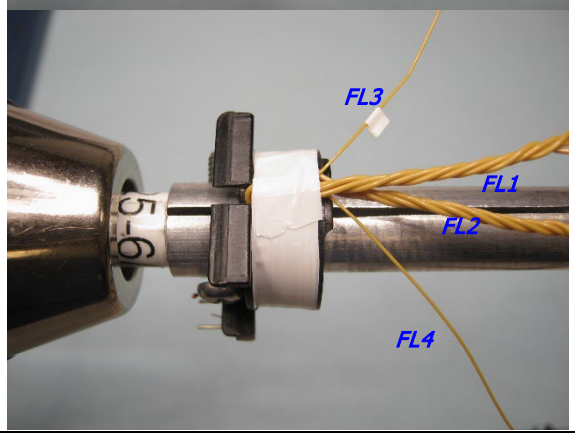
	 	
Insulation		1 layer of tape item [7].
WD2: Bias **&** **WD3: Shield1**		Use 1 wire item [4] start at pin 5 for Bias winding, also use 2 wires same item [4] start at pin 3 for Shield1 winding. Wind all 3 wires in parallel, at the 9th turn, place a piece of tape to hold the wires, bring 1 wire of Bias winding to the left and terminate at pin 3. Continue winding to 12th turn, cut short 2 wires for

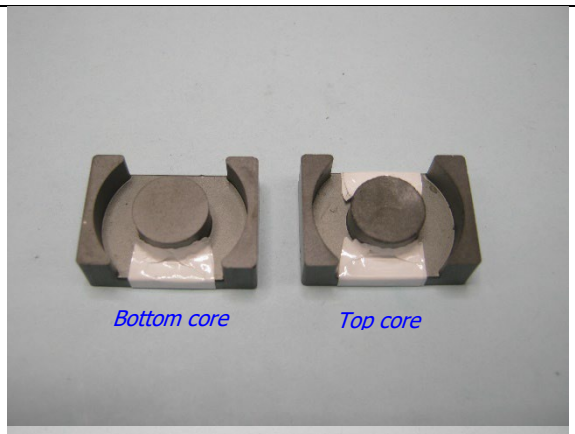
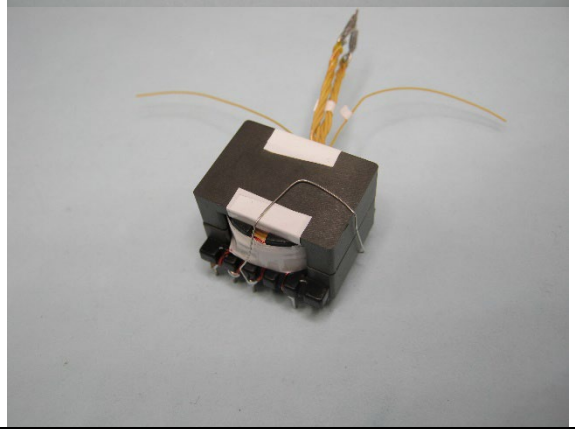
	  	Shield1 Winding as No-Connect.
Insulation		1 layer of tape item [7].

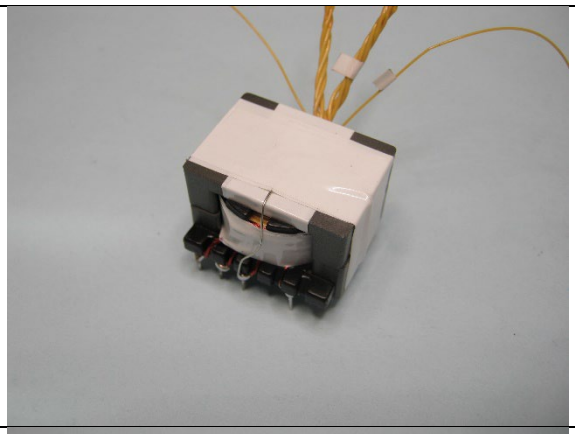
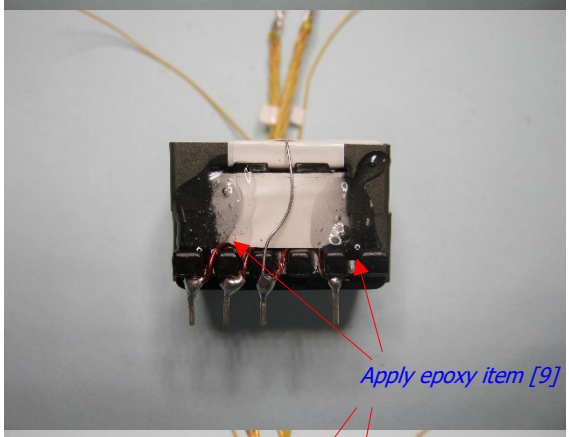
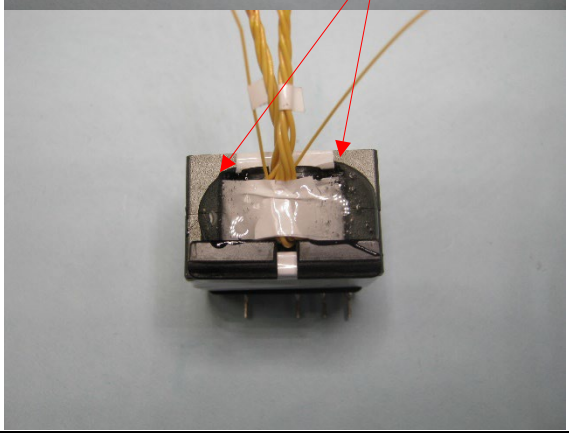
WD4 **Secondary**	   	Start at left slot of secondary side, use 2 wires item [5], leaving ~ 40.0 mm floating, and mark as FL1.Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0 mm floating, and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.

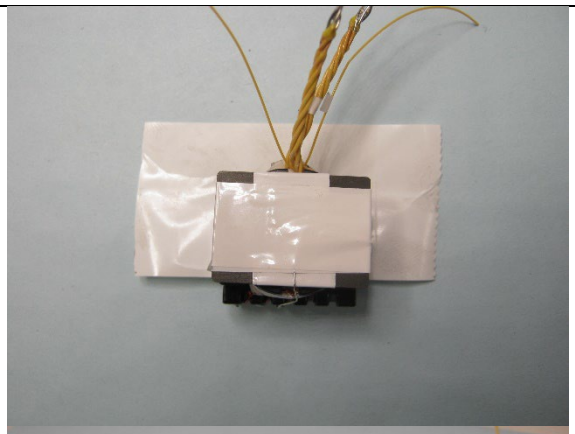
WD5 **Secondary Bias**	 	Also start at left slot of secondary, use 1 wire item [6], wind 2 turns with the same way above, start lead FL3 and end lead FL4
Insulation		1 layer of tape item [7].
WD6 **Shield 2**		Use 3 wires item [4], start at right with floating ~ 30mm, wind 11 turns from right to left. At the last turn cut short as No-Connect NC, then bring floating wires back to the left and terminate at pin 1.

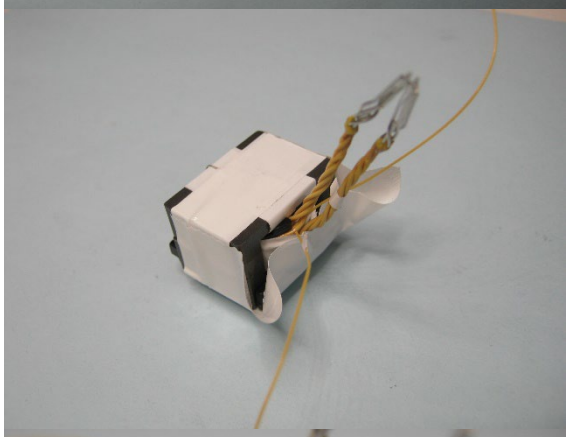
		
Insulation		1 layer of tape item [7].
WD7 **2nd Primary**		Use floating wire from WD1-1st Primary, wind 11 turns from left to right. At the last turn, bring the wire back to the left and terminate at pin 1.

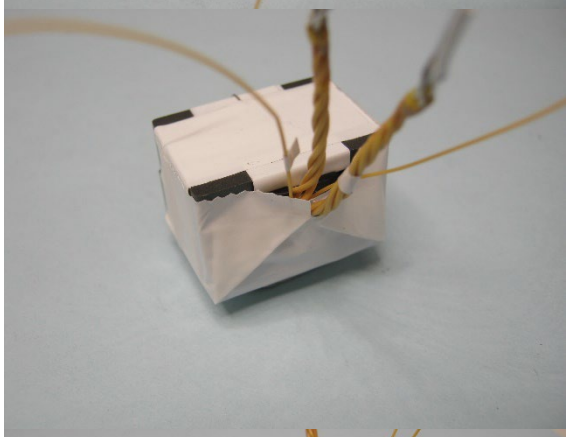
	 	
Insulation	 	1 layer of tape item [7], bring wires FL1 & FL3 from the left to the right and continue with 2 layers of tape to secure all windings and wires.

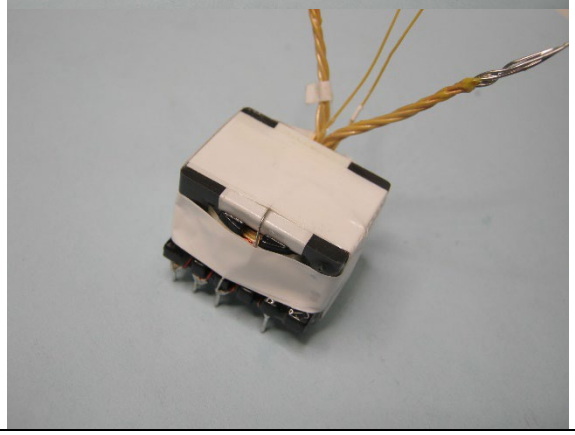
Finish	 *Bottom core* *Top core*  *Glue item [10]*  	Gap cores to get 640uH. Apply 2 layers of tape item [8] onto core sides, *(see pictures beside).* Apply glue item [10] at center legs of cores. Solder pin 3 with bus-wire item [9] then lean along core halves and secure with tape. Apply epoxy item [12] between cores to body on top and bottom of the transformer. *(see pictures below).* Varnish with item [13]. Place 2 layers of tape item [11] at the bottom then wrap up to the body of transformer, and tape around 1layer of tape item [7]. (*See pictures below*).

		
Finish (continued)	 *Epoxy item [12]*  	Apply epoxy item [12] between cores to body on top and bottom of the transformer. *(see pictures below).* Varnish with item [13]. Place 2 layers of tape item [11] at the bottom then wrap up to the body of transformer, and tape around 1layer of tape item [7]. (*See pictures below*).









8 Common Mode Choke Specifications

8.1 730 µH Common Mode Choke (L2)

8.1.1 Electrical Diagram

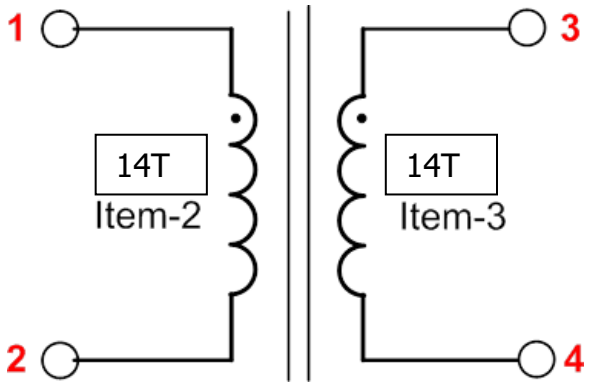


Figure 11 – Inductor Electrical Diagram.

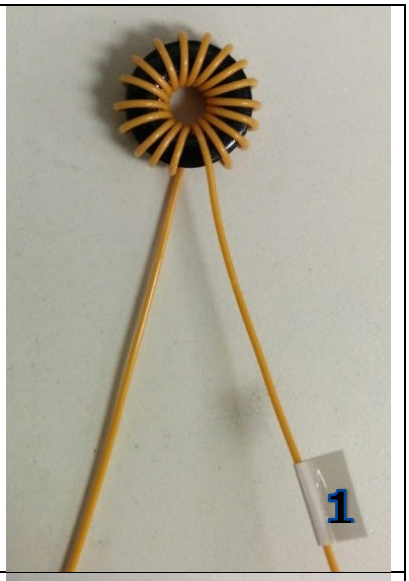
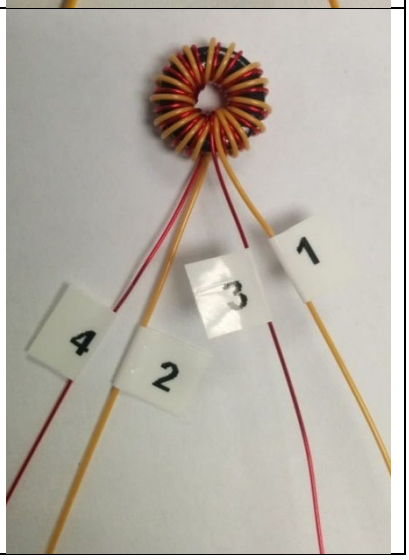
8.1.2 Electrical Specifications

Inductance	Pin 1 – pin 2 (pin 3 – pin 4), all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	≥730 µH

8.1.3 Material List

Item	Description
[1]	Toroidal Core: PI#: 32-00330-00.
[2]	Triple Insulated Wire: #25 AWG, Triple Coated.
[3]	Magnet Wire: #25 AWG, Double Coated.

8.1.4 Winding Instructions

Mark the start end of the winding as 1 and wind 14 turns of Item [2] on Item [1]. Mark the end of this winding as 2	
Repeat the same procedure as above for the other winding using Item [3], making sure that the start/end and the direction of winding is the same as the first winding. Varnish using Item [4]. Mark the start of this winding as 3 and the end as 4.	

9 Transformer Design Spreadsheet

1	ACDC_InnoSwitch4-CZ_USBPD_ Flyback_052722; Rev.3.3; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4-CZ USB-PD Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN			90	V	Minimum AC input voltage
5	VIN_MAX			265	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Input voltage range
7	FLINE	47		47	Hz	AC Input voltage frequency
8	CAP_INPUT	122.0		122.0	uF	Input capacitance
9						
10	**SET-POINT 1**					
11	VOUT1	20.00		20.00	V	Output voltage 1, should be the highest output voltage required
12	IOUT1	3.000		3.000	A	Output current 1
13	POUT1			60.00	W	Output power 1
14	EFFICIENCY1	0.93		0.93		Converter efficiency for output 1
15	Z_FACTOR1	0.50		0.50		Z-factor for output 1
16	TYPE	APDO	Info	APDO		The voltage entered is a standard PDO(Power Delivery Object)
17						
18	**SET-POINT 2**					
19	VOUT2	15.00		15.30	V	Output voltage 2
20	IOUT2	3.000		3.000	A	Output current 2
21	POUT2			45.90	W	Output power 2
22	EFFICIENCY2	0.93		0.93		Converter efficiency for output 2
23	Z_FACTOR2	0.50		0.50		Z-factor for output 2
24	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
25						
26	**SET-POINT 3**					
27	VOUT3	9.00		9.30	V	Output voltage 3
28	IOUT3	3.000		3.000	A	Output current 3
29	POUT3			27.90	W	Output power 3
30	EFFICIENCY3	0.92		0.92		Converter efficiency for output 3
31	Z_FACTOR3	0.50		0.50		Z-factor for output 3
32	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
33						
34	**SET-POINT 4**					
35	VOUT4	5.00		5.30	V	Output voltage 4
36	IOUT4	3.000		3.000	A	Output current 4
37	POUT4			15.90	W	Output power 4
38	EFFICIENCY4	0.91		0.91		Converter efficiency for output 4
39	Z_FACTOR4	0.50		0.50		Z-factor for output 4
40	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
41						
42	**SET-POINT 5**					
43	VOUT5	3.30		3.60	V	Output voltage 5
44	IOUT5	3.000		3.000	A	Output current 5
45	POUT5			10.80	W	Output power 5
46	EFFICIENCY5	0.90		0.90		Converter efficiency for output 5
47	Z_FACTOR5	0.50		0.50		Z-factor for output 5
48	TYPE	PDO	Info	PDO		The voltage entered is not a standard PDO(Power Delivery Object)

49						
81						
82	VOLTAGE_CDC	0.300		0.300	V	Cable drop compensation desired at full load
83						
84						
85						
86	**PRIMARY CONTROLLER SELECTION**					
87	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
88	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
89	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
90	DEVICE_GENERIC	INN4373F		INN4373F		Generic device code
91	DEVICE_CODE			INN4373F		Device code
92	PDEVICE_MAX			60	W	Device maximum power capability
93	RDSON_100DEG			1.02	Ω	Primary switch on-time resistance at 100°C
94	ILIMIT_MIN			1.581	A	Primary switch minimum current limit
95	ILIMIT_TYP			1.700	A	Primary switch typical current limit
96	ILIMIT_MAX			1.819	A	Primary switch maximum current limit
97	VDRAIN_ON_PRSW			0.72	V	Primary switch on-time voltage drop
98	VDRAIN_OFF_PRSW			563.31	V	Peak drain voltage on the primary switch during turn-off
99						
100						
101						
102	**WORST CASE ELECTRICAL PARAMETERS**					
103	FSWITCHING_MAX	102642	Info	102642	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
104	VOR	140.0		140.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
105	VMIN			88.66	V	Valley of the rectified minimum input AC voltage at full load
106	KP			0.535		Measure of continuous/discontinuous mode of operation
107	MODE_OPERATION			CCM		Mode of operation
108	DUTYCYCLE			0.614		Primary switch duty cycle
109	TIME_ON			11.43	us	Primary switch on-time
110	TIME_OFF			3.26	us	Primary switch off-time
111	LPRIMARY_MIN			608.0	uH	Minimum primary magnetizing inductance
112	LPRIMARY_TYP			640.0	uH	Typical primary magnetizing inductance
113	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
114	LPRIMARY_MAX			672.0	uH	Maximum primary magnetizing inductance
115						
116	**PRIMARY CURRENT**					
117	IAVG_PRIMARY			0.708	A	Primary switch average current
118	IPEAK_PRIMARY			1.757	A	Primary switch peak current
119	IPEDESTAL_PRIMARY			0.731	A	Primary switch current pedestal
120	IRIPPLE_PRIMARY			1.556	A	Primary switch ripple current
121	IRMS_PRIMARY			0.944	A	Primary switch RMS current
122						
123	**SECONDARY CURRENT**					
124	IPEAK_SECONDARY			12.298	A	Secondary winding peak current
125	IPEDESTAL_SECONDARY			5.119	A	Secondary winding pedestal current
126	IRMS_SECONDARY			5.236	A	Secondary winding RMS current
127	IRIPPLE_CAP_OUT			4.292	A	Output capacitor ripple current
128						
129						
130						
131	**TRANSFORMER CONSTRUCTION PARAMETERS**					
132	**CORE SELECTION**					
133	CORE	EQ25		EQ25		Core selection. Refer to the "Transformer Construction" tab for the detailed report.
134	CORE NAME			EQ25-3C95		Core code

135	AE			100.0	mm^2	Core cross sectional area
136	LE			41.4	mm	Core magnetic path length
137	AL			5710	nH	Ungapped core effective inductance per turns squared
138	VE			4145	mm^3	Core volume
139	BOBBIN NAME			TBI-235-01091.1206		Bobbin name
140	AW			34.8	mm^2	Bobbin window area
141	BW			8.10	mm	Bobbin width
142	MARGIN			0.0	mm	Bobbin safety margin
143						
144	**PRIMARY WINDING**					
145	NPRIMARY			35		Primary winding number of turns
146	BPEAK			3642	Gauss	Peak flux density
147	BMAX			3340	Gauss	Maximum flux density
148	BAC			1467	Gauss	AC flux density (0.5 x Peak to Peak)
149	ALG			522	nH	Typical gapped core effective inductance per turns squared
150	LG			0.219	mm	Core gap length
151						
152	**PRIMARY BIAS WINDING**					
153	NBIAS_PRIMARY			9		Primary bias winding number of turns
154						
155	**SECONDARY WINDING**					
156	NSECONDARY	5		5		Secondary winding number of turns
157						
158	**SECONDARY BIAS WINDING**					
159	NBIAS_SECONDARY			2		Secondary bias winding number of turns
160						
161						
162	**PRIMARY COMPONENTS SELECTION**					
163	CLAMPZERO					
164	LLEAK	6.50		6.50	uH	Primary winding leakage inductance
165	CCLAMP			100.0	nF	Primary clamp capacitor
166	RD_CLAMPZERO	30		30	kΩ	HSD resistor
167	TLLDL/THLDL			120.0	ns	HSD resistor programmed delay
168	TIME_CLAMPZERO_OFF_TO_PRIMARY_ON			65.0	ns	Time between the ClampZero FET turn off and the primary FET turns on based on the HSD resistor selection
169	TIME_VDS_VALLEY			49.6	ns	Time taken by the VDS ring to reach its first valley
170	IPEAK_CLAMPZERO			1.711	A	Active clamp peak current
171						
172	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
173	BROWN-IN REQURED	76.00		76.00	V	Required AC RMS/DC line brown-in threshold
174	RLS			3.82	MΩ	Connect two 1.91 MOhm resistors to the V-pin for the required UV/OV threshold
175	BROWN-IN ACTUAL			76.58	V	Actual AC RMS/DC brown-in threshold using standard resistors
176	BROWN-OUT ACTUAL			69.26	V	Actual AC RMS/DC brown-out threshold using standard resistors
177	OVERVOLTAGE_LINE			322.38	V	Actual AC RMS/DC line over-voltage threshold
178						
179	PRIMARY BIAS WINDING					
180	VBIAS_PRIMARY	8.00	Info	8.00	V	The rectified primary bias voltage maybe too low to supply the BPP pin: Increase the rectified primary bias voltage to a value higher than 9V
181	VF_BIAS_PRIMARY			0.70	V	Primary bias winding diode forward drop
182	VREVERSE_BIASDIODE_PRIMARY			131.99	V	Primary bias diode reverse voltage (not accounting parasitic voltage ring)

183	CBIAS_PRIMARY			22	uF	Primary bias winding rectification capacitor
184	CBPP			0.47	uF	BPP pin capacitor
185						
186						
187						
188	**SECONDARY COMPONENTS SELECTION**					
189	RECTIFIER					
190	VDRAIN_OFF_SRFET			73.54	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
191	SRFET	AUTO		SiR878ADP		Secondary rectifier (Logic MOSFET)
192	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
193	RDSON_SRFET			18.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
194						
195	**SECONDARY BIAS WINDING**					
196	USE_SECONDARY_BIAS	AUTO		YES		Use secondary bias winding for the design
197	VBIAS_SECONDARY			6.00	V	Rectified secondary bias voltage at full load
198	VF_BIAS_SECONDARY			0.70	V	Secondary bias winding diode forward drop
199	VREVERSE_BIASDIODE_SECONDARY			112.66	V	Secondary bias diode reverse voltage (not accounting parasitic voltage ring)
200	CBIAS_SECONDARY			10	uF	Secondary bias winding rectification capacitor
201	CBPS			2.20	uF	BPS pin capacitor

NOTE: Even though PIXls suggests using SiR878ADP as SR FET, AON6220 has been used in the design

10 Performance Data

Note 1: Output voltages measured on board
2: Measurements taken at room temperature (approximately 24 °C)

10.1 No-Load Input Power at 5 VOUT

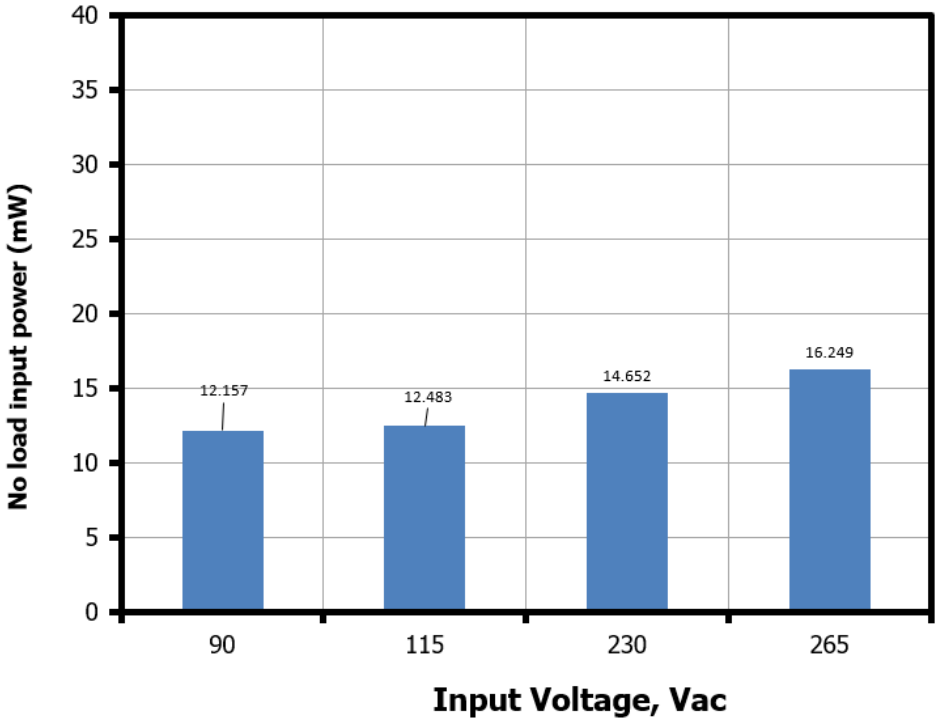


Figure 12 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

10.2 Full Load Efficiency

V_{OUT} (V)	Load (A)	Power (W)	Full Load Efficiency (%)			
			90 VAC	115 VAC	230 VAC	265 VAC
5	3	15	91.31	91.85	91.86	91.51
9	3	27	92.09	92.50	93.26	93.03
15	3	45	92.31	92.59	93.90	93.83
20	3	60	91.86	92.82	93.99	94.07

10.3 Average and 10% Load Efficiency (on Board)

10.3.1 Efficiency Requirements

V_{OUT} (V)	Model (V)	Test Effective Power (W)	Average 2016 New EISA2007	Average Jan-16 CoC v5 Tier 2	10% Load Jan-16 CoC v5 Tier 2
5	<6	15	81.4%	81.8%	72.5%
9	>6	27	86.6 %	87.3%	77.3%
15	>6	45	87.7%	88.9%	78.9%
20	>6	60	88.0%	89.0%	79.0%

10.3.2 Efficiency Performance Summary (on Board)

V_{OUT} (V)	Current (A)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	3	92.27	91.06	89.68	85.83
9	3	92.66	92.72	90.92	87.61
15	3	92.70	93.48	89.71	88.99
20	3	92.51	93.68	89.29	89.38

10.3.3 Average and 10% Load Efficiency at 115 VAC (on Board)

10.3.3.1 Output: 5 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	5.23	2.99	91.85	**92.27**
75	5.17	2.25	92.14	
50	5.12	1.50	92.32	
25	5.07	0.75	92.76	
10	5.04	0.30	**89.68**	

10.3.3.2 Output: 9 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	9.23	3.00	92.50	**92.66**
75	9.18	2.25	92.75	
50	9.13	1.50	92.81	
25	9.07	0.75	92.57	
10	9.04	0.30	**90.92**	

10.3.3.3 Output: 15 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.25	3.00	92.59	**92.70**
75	15.20	2.25	92.82	
50	15.15	1.50	92.87	
25	15.09	0.75	92.52	
10	15.05	0.30	**89.71**	

10.3.3.4 Output: 20 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	20.26	3.00	92.82	**92.50**
75	20.22	2.25	92.29	
50	20.15	1.50	92.68	
25	20.10	0.75	92.25	
10	20.05	0.30	**89.29**	

10.3.4 Average and 10% Load Efficiency at 230 VAC (on Board)

10.3.4.1 Output: 5 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	5.24	2.99	91.86	**91.06**
75	5.18	2.25	91.83	
50	5.13	1.50	91.28	
25	5.07	0.75	89.28	
10	5.04	0.30	**85.83**	

10.3.4.2 Output: 9 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	9.24	3	93.26	**92.72**
75	9.19	2.25	93.21	
50	9.13	1.5	92.96	
25	9.07	0.75	91.44	
10	9.04	0.3	**87.61**	

10.3.4.3 Output: 15 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.25	3.00	93.90	**93.48**
75	15.20	2.25	93.86	
50	15.14	1.50	93.66	
25	15.09	0.75	92.49	
10	15.05	0.30	**88.99**	

10.3.4.4 Output: 20 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	20.26	2.99	93.99	**93.68**
75	20.22	2.25	94.02	
50	20.15	1.50	93.82	
25	20.10	0.75	92.89	
10	20.05	0.30	**89.38**	

10.4 Efficiency Across Line (on Board)

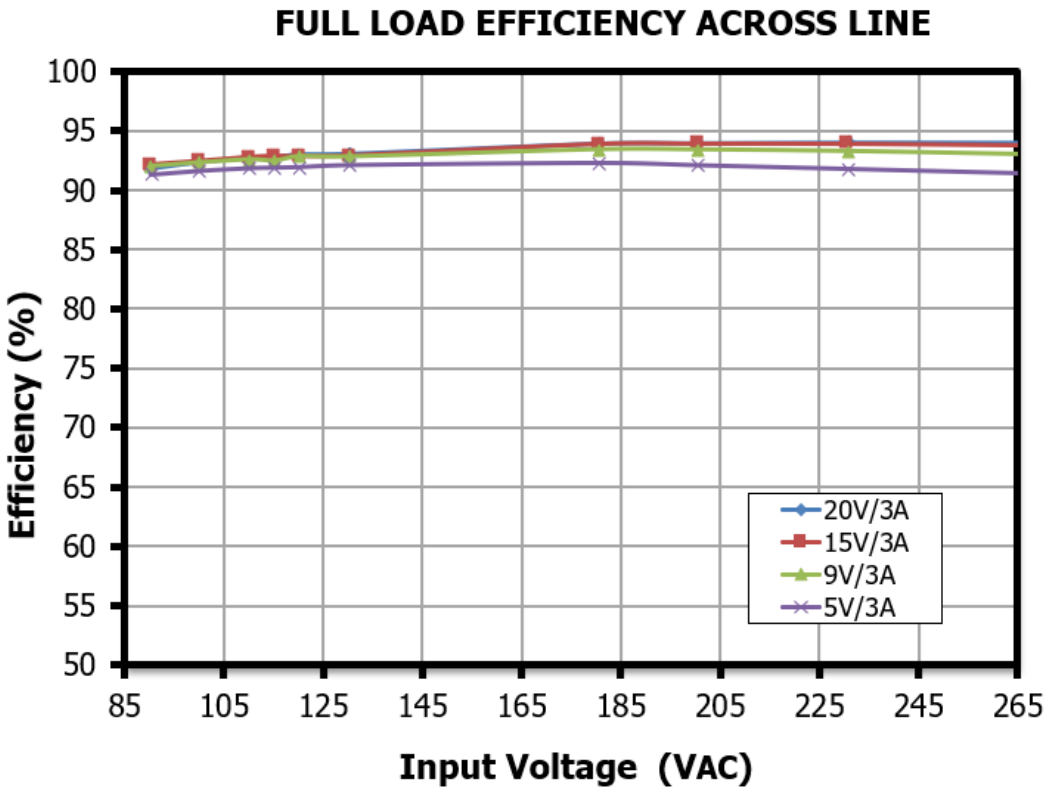


Figure 13 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, and 20 V Output, Room Temperature.

10.5 Line Regulation (on Board)

Note: CDC used for all output voltage conditions = 300 mV

10.5.1 Output: 5 V / 3 A

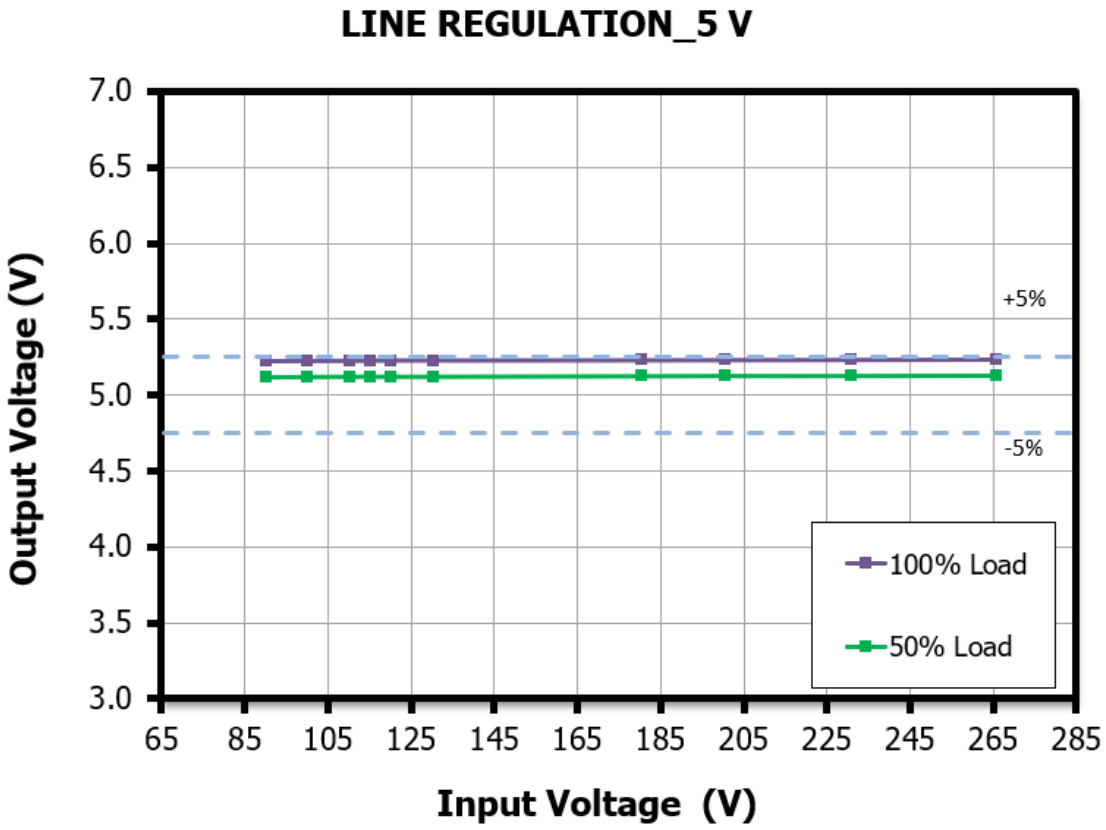


Figure 14 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

10.5.2 Output: 9 V / 3 A

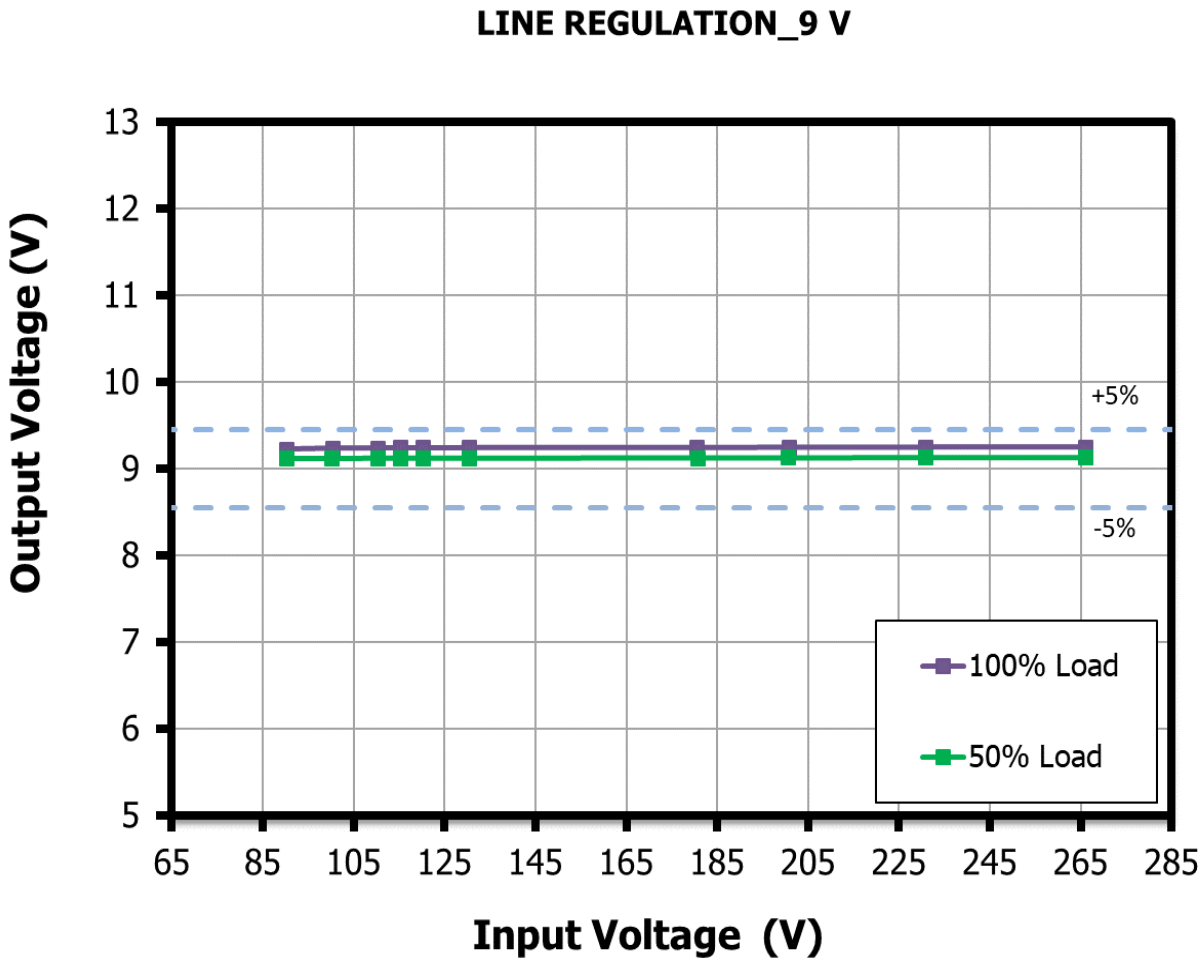


Figure 15 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

10.5.3 Output: 15 V / 3 A

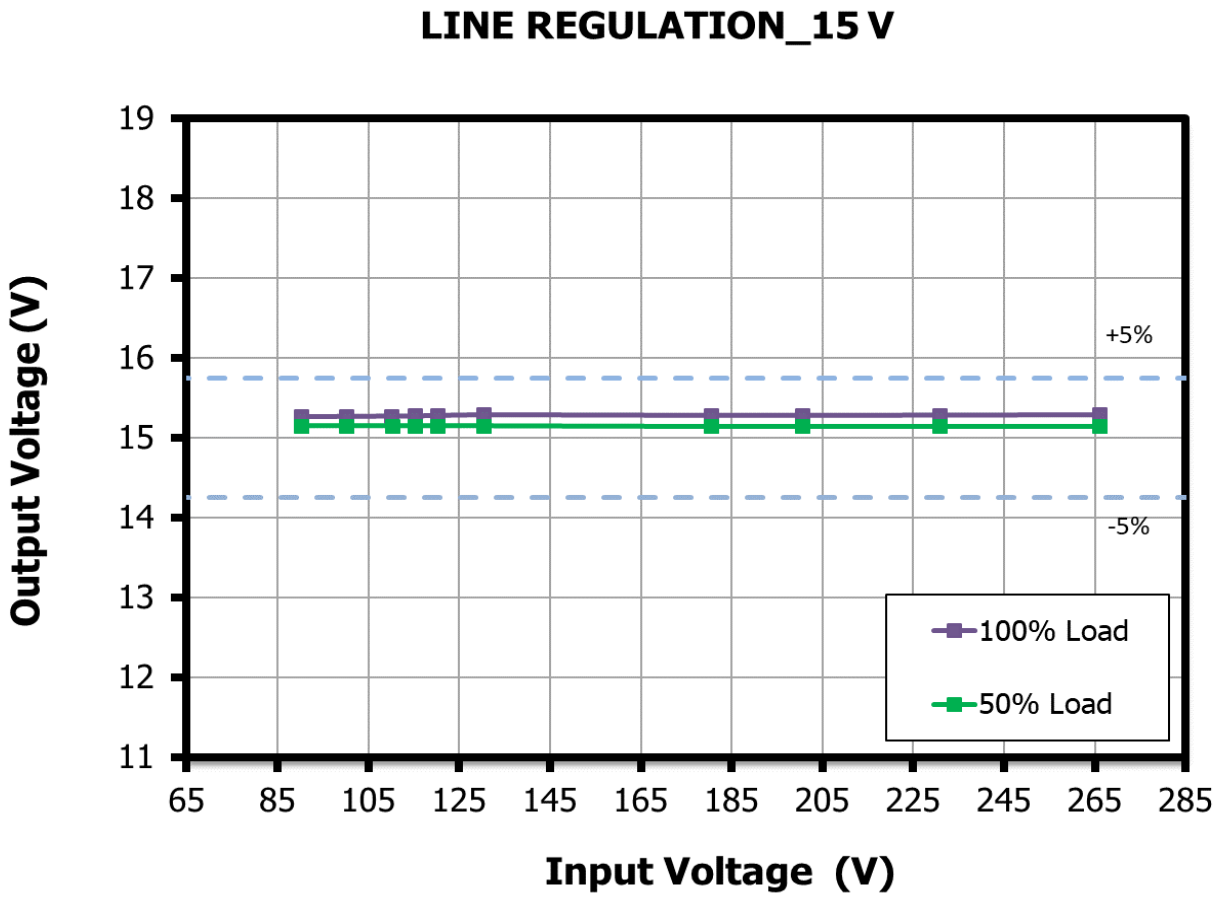


Figure 16 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

10.5.4 Output: 20 V / 3 A

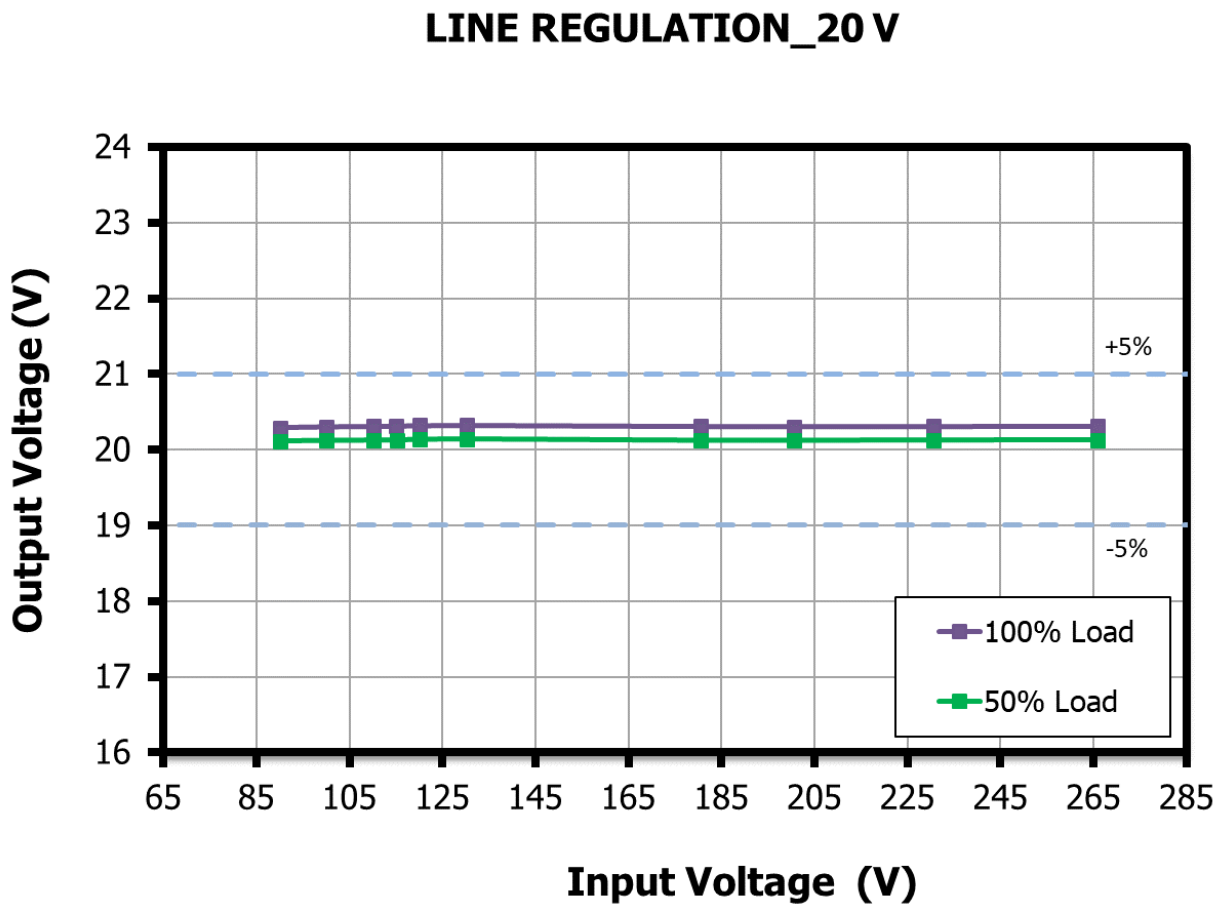


Figure 17 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

10.6 Load Regulation (on Board)

Note: This design demonstrates the InnoSwitch4-Pro CDC feature (set to 300 mV). CDC setting can be adjusted through I^2C to meet target performance, such as USB PD Specifications acceptable voltage range for 5 V operation, vSafe5V (4.75 V to 5.5 V, measured on-board).

10.6.1 Output: 5 V / 3 A

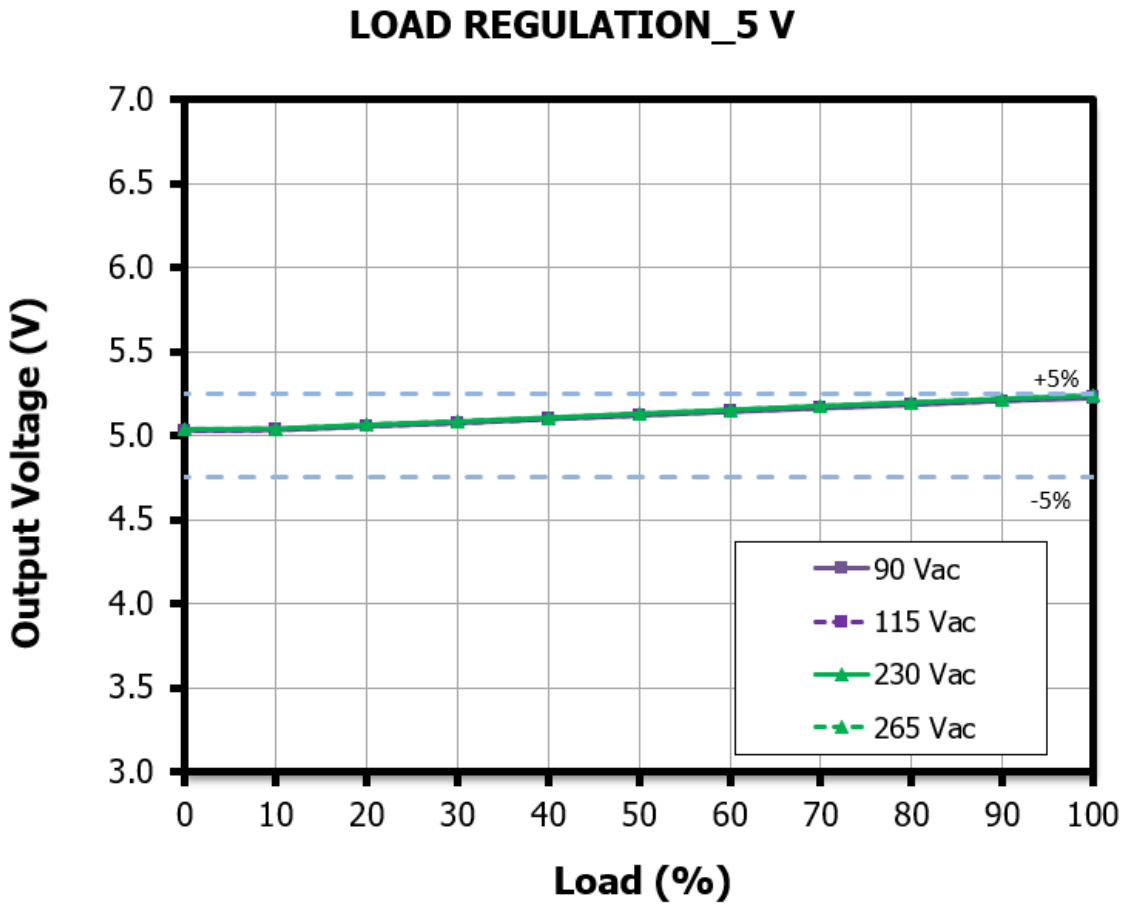


Figure 18 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

10.6.2 Output: 9 V / 3 A

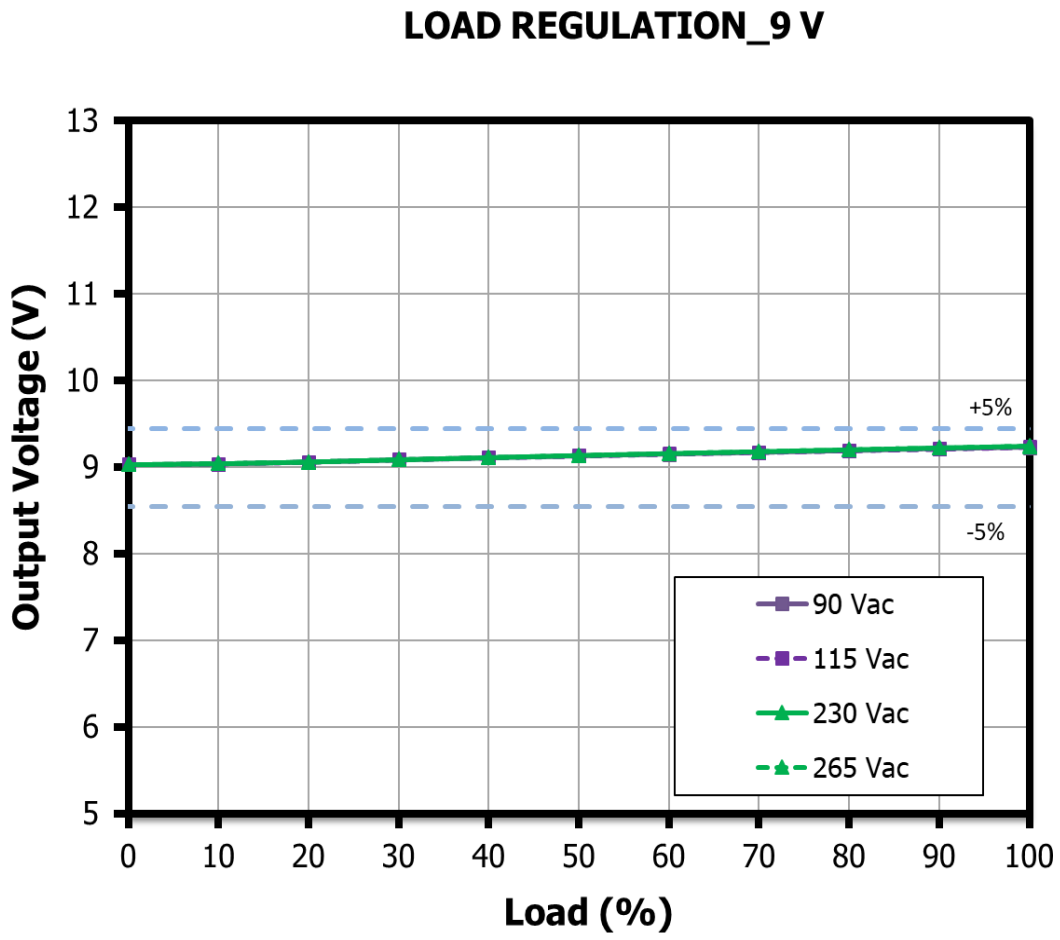


Figure 19 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

10.6.3 Output: 15 V / 3 A

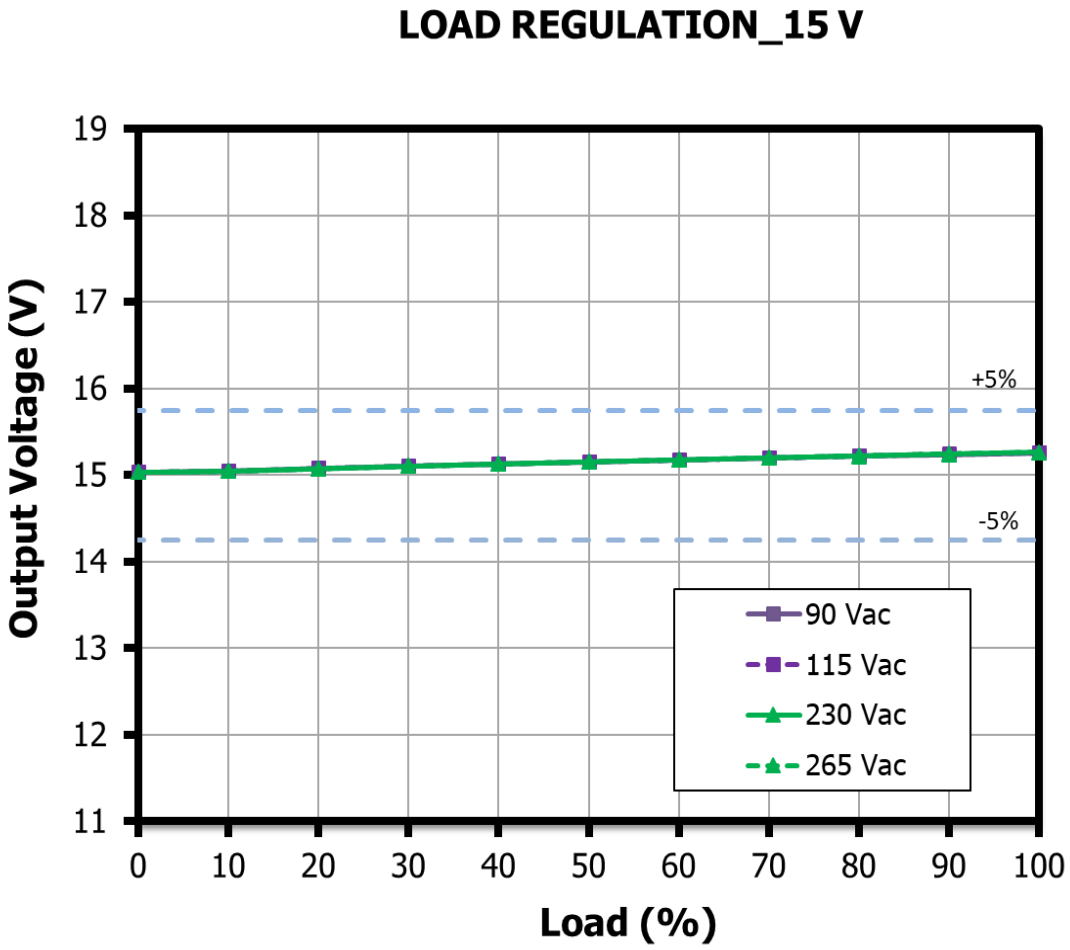


Figure 20 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

10.6.4 Output: 20 V / 3 A

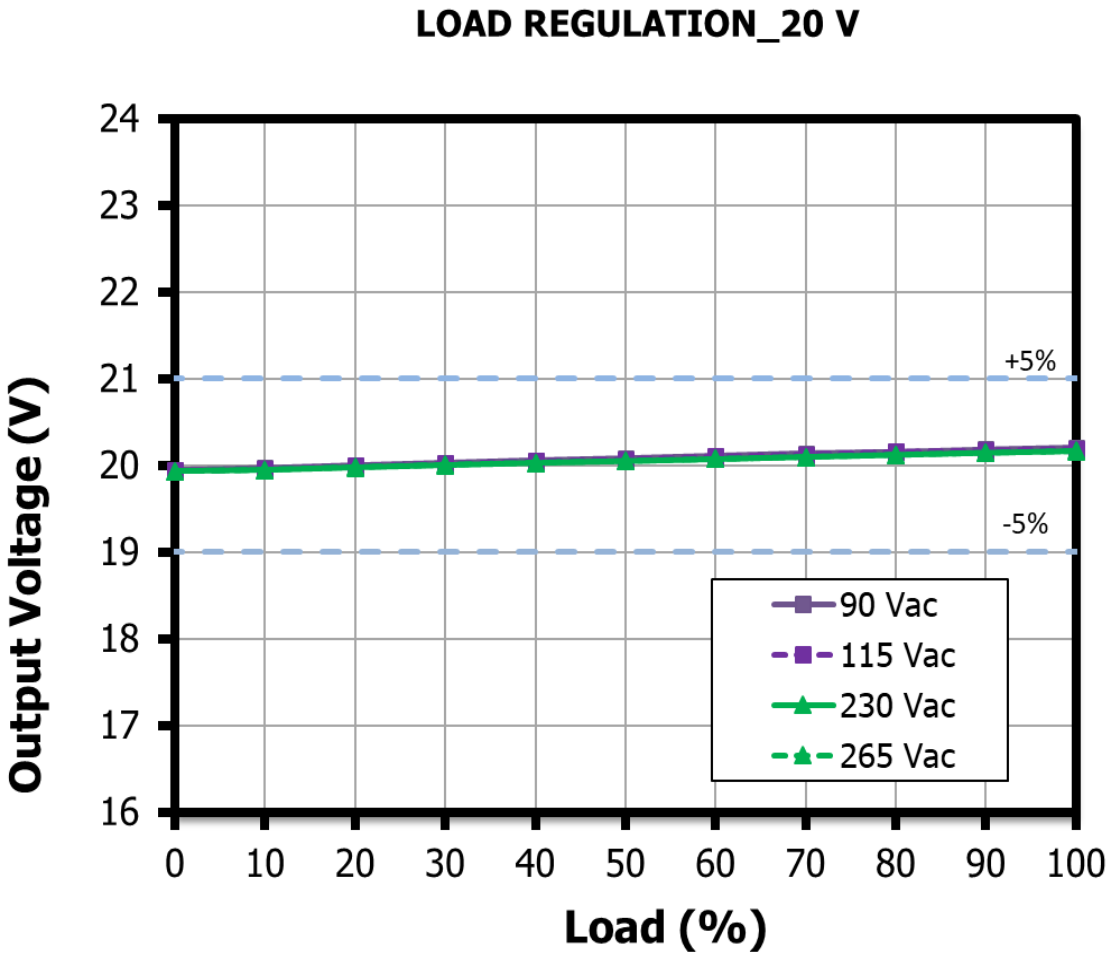


Figure 21 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

11 Thermal Performance in Open Case

Note: The performance data below is for open case operation under room temperature with two-hours soak for each condition

11.1 Output: 5 V / 3 A (90 VAC)

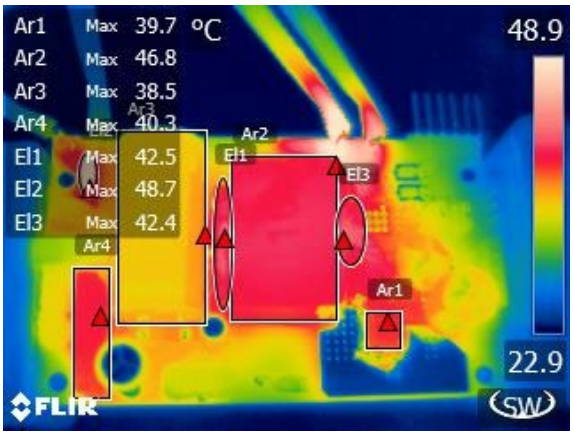


Figure 22 – Top Thermal Image.
Ar1: SR FET = 39.7ºC.
Ar2: Transformer core, T1 = 46.8 ºC.
Ar3: Bulk Cap = 38.5 ºC.
Ar4: Bridge Rectifier = 40.3 ºC.
El1: Transformer Winding = 42.5 ºC.
El2: Thermistor, RT1= 48.7 ºC.
Ambient: = 26.3 ºC.

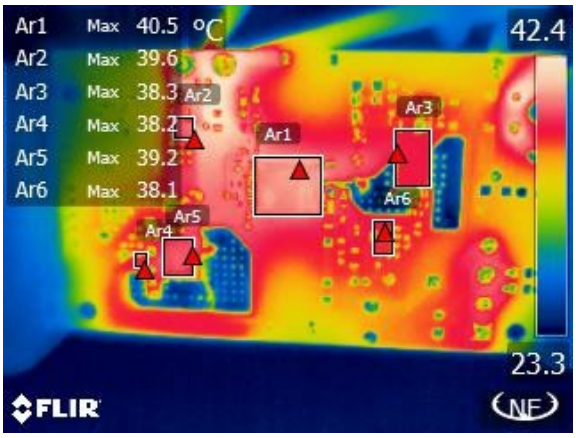


Figure 23 – Bottom Thermal Image.
Ar1: InnoSwitch4-Pro, U2 = 40.5 ºC.
Ar2: Bus Switch, Q3 =39.6 ºC.
Ar3: Clamp Zero IC = 38.3 ºC.
Ar4: Sec. Snubber Diode = 38.2 ºC.
Ar5: Sec. Schottky Diode = 39.2 ºC.
Ar6: BJT, Q1 = 38.1 ºC.

11.2 Output: 5 V / 3 A (265 VAC)

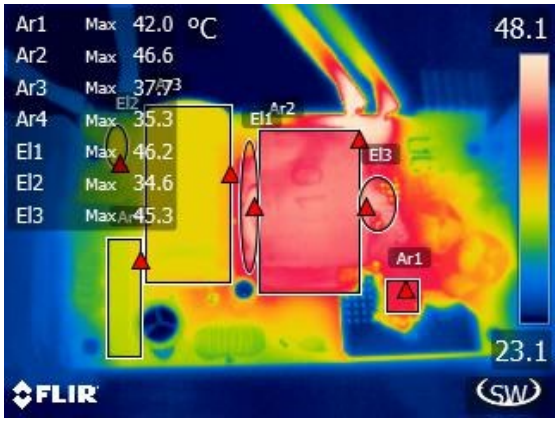


Figure 24 – Top Thermal Image.
Ar1: SR FET = 42 ºC.
Ar2: Transformer core, T1 = 46.6 ºC.
Ar3: Bulk Cap = 37.7 ºC.
Ar4: Bridge Rectifier = 35.3 ºC.
El1: Transformer Winding = 46.2 ºC.
El2: Thermistor, RT1= 34.6 ºC.
Ambient: = 25.4 ºC.

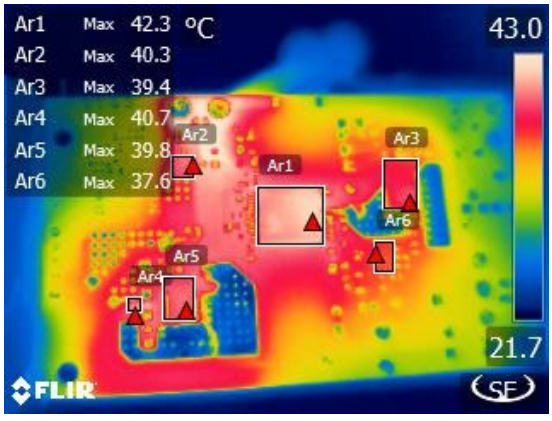


Figure 25 – Bottom Thermal Image.
Ar1: InnoSwitch4-Pro, U2 = 42.3 ºC.
Ar2: Bus Switch, Q3 = 40.3 ºC.
Ar3: Clamp Zero IC = 39.4 ºC.
Ar4: Sec. Snubber Diode = 40.7 ºC.
Ar5: Sec. Schottky Diode = 39.8 ºC.
Ar6: BJT, Q1 = 37.6 ºC.

11.3 Output: 9 V / 3 A (90 VAC)

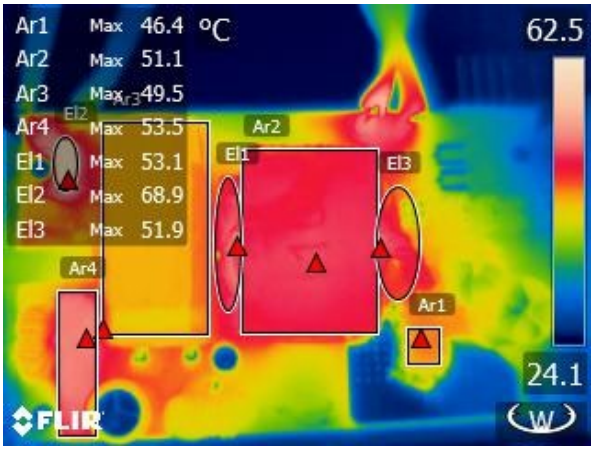


Figure 26 – Top Thermal Image.
Ar1: SR FET = 46.4 ºC.
Ar2: Transformer core, T1 = 51.1 ºC.
Ar3: Bulk Cap = 49.5 ºC.
Ar4: Bridge Rectifier = 53.5 ºC.
El1: Transformer Winding = 53.1 ºC.
El2: Thermistor, RT1= 68.9 ºC.
Ambient: = 28.2 ºC.

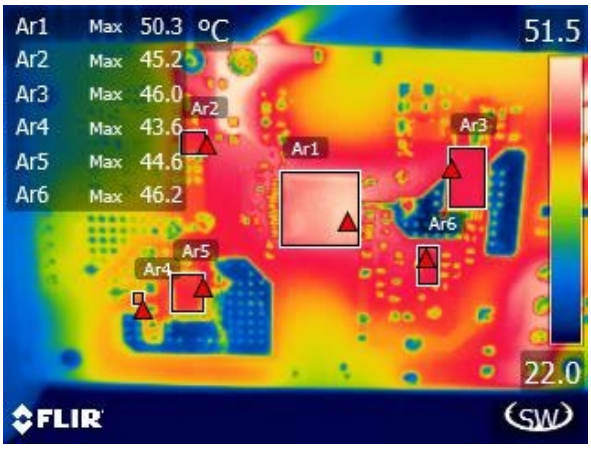


Figure 27 – Bottom Thermal Image.
Ar1: InnoSwitch4-Pro, U2 = 50.3 ºC.
Ar2: Bus Switch, Q3 = 45.2 ºC.
Ar3: Clamp Zero IC = 46 ºC.
Ar4: Sec. Snubber Diode = 43.6 ºC.
Ar5: Sec. Schottky Diode = 44.6 ºC.
Ar6: BJT, Q1 = 46.2ºC.

11.4 Output: 9 V / 3 A (265 VAC)

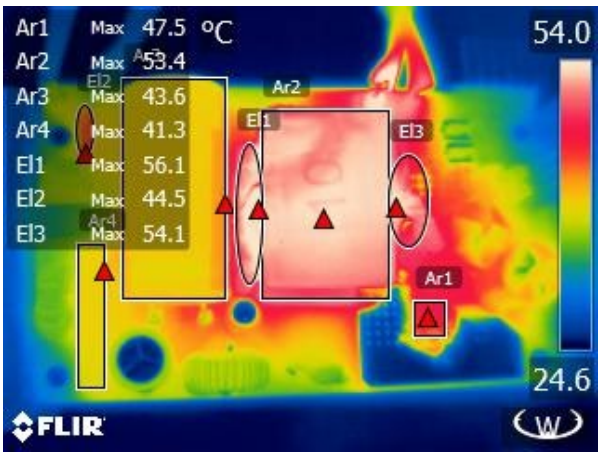


Figure 28 – Top Thermal Image.
Ar1: SR FET = 47.5 ºC.
Ar2: Transformer core, T1 = 53.4 ºC.
Ar3: Bulk Cap = 43.6 ºC.
Ar4: Bridge Rectifier = 41.3 ºC.
El1: Transformer Winding = 56.1 ºC.
El2: Thermistor, RT1= 44.5 ºC.
Ambient: = 27.2 ºC.

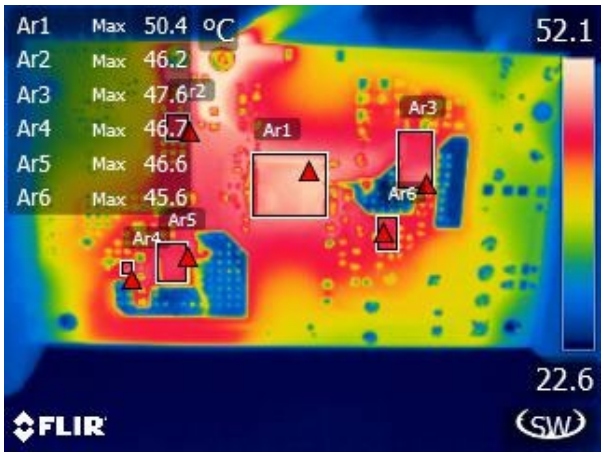


Figure 29 – Bottom Thermal Image.
Ar1: InnoSwitch4-Pro, U2 = 50.4 ºC.
Ar2: Bus Switch, Q3 = 46.2 ºC.
Ar3: Clamp Zero IC = 47.6 ºC.
Ar4: Sec. Snubber Diode = 46.7 ºC.
Ar5: Sec. Schottky Diode = 46.6 ºC.
Ar6: BJT, Q1 = 45.6 ºC.

11.5 Output: 15 V / 3 A (90 VAC)

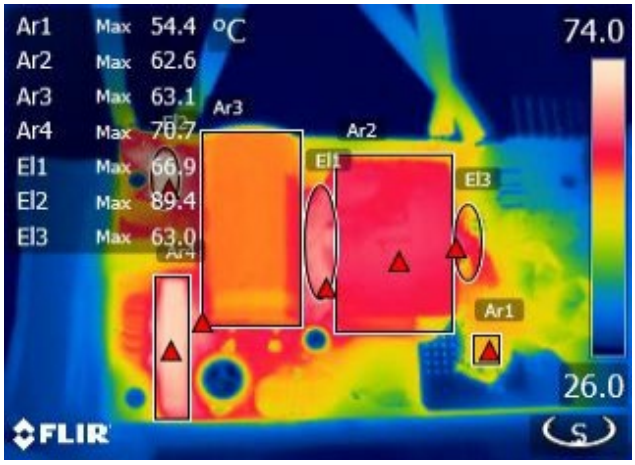


Figure 30 – Top Thermal Image.
Ar1: SR FET = 54.4 ºC.
Ar2: Transformer core, T1 = 62.6 ºC.
Ar3: Bulk Cap = 63.1 ºC.
Ar4: Bridge Rectifier = 70.7 ºC.
El1: Transformer Winding = 66.9 ºC.
El2: Thermistor, RT1= 89.4 ºC.
Ambient: = 28.7 ºC.

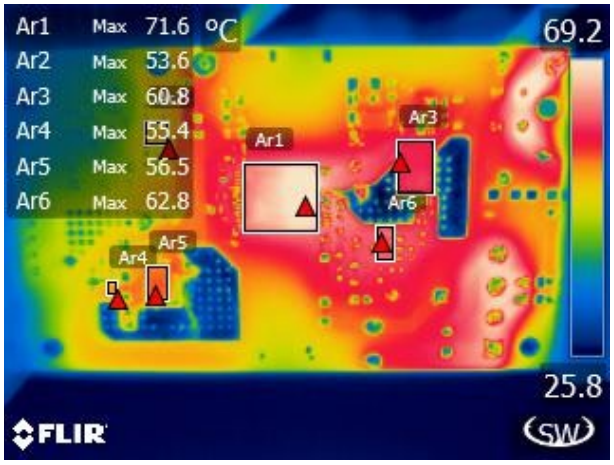


Figure 31 – Bottom Thermal Image.
Ar1: InnoSwitch4-Pro, U2 = 71.6 ºC.
Ar2: Bus Switch, Q3 = 53.6 ºC.
Ar3: Clamp Zero IC = 60.8 ºC.
Ar4: Sec. Snubber Diode = 55.4 ºC.
Ar5: Sec. Schottky Diode = 56.5 ºC.
Ar6: BJT, Q1 = 62.8 ºC.

11.6 Output: 15 V / 3 A (265 VAC)

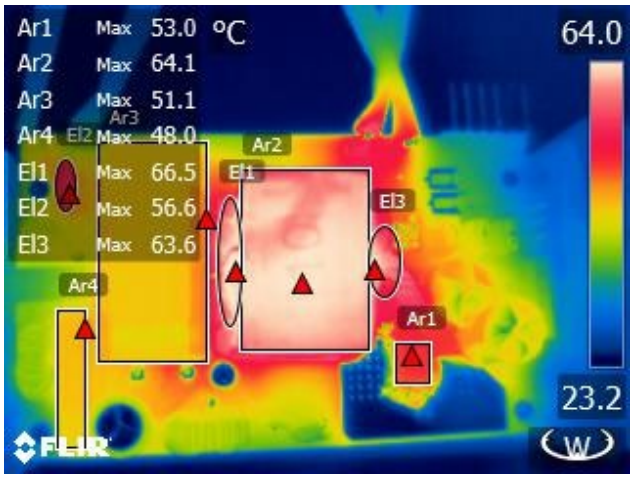


Figure 32 – Top Thermal Image.
Ar1: SR FET = 53 ºC.
Ar2: Transformer core, T1 = 64.1 ºC.
Ar3: Bulk Cap = 51.1 ºC.
Ar4: Bridge Rectifier = 48 ºC.
El1: Transformer Winding = 66.5 ºC.
El2: Thermistor, RT1= 56.6 ºC.
Ambient: = 25.9 ºC.

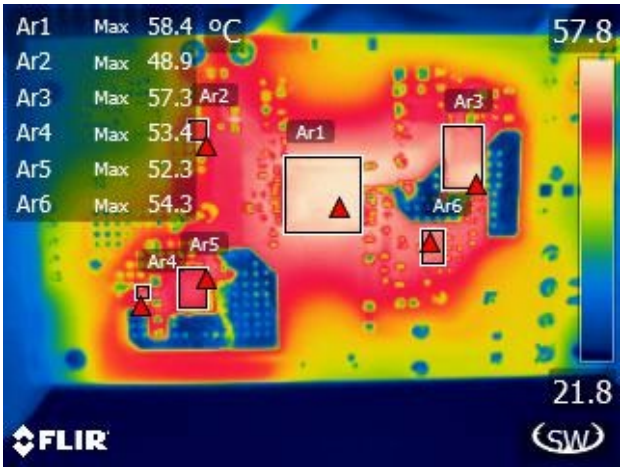


Figure 33 – Bottom Thermal Image.
Ar1: InnoSwitch4-Pro, U2 = 58.4 ºC.
Ar2: Bus Switch, Q3 = 48.9 ºC.
Ar3: Clamp Zero IC = 57.3 ºC.
Ar4: Sec. Snubber Diode = 53.4 ºC.
Ar5: Sec. Schottky Diode = 52.3 ºC.
Ar6: BJT, Q1 = 54.3 ºC.

11.7 Output: 20 V / 3 A (90 VAC)

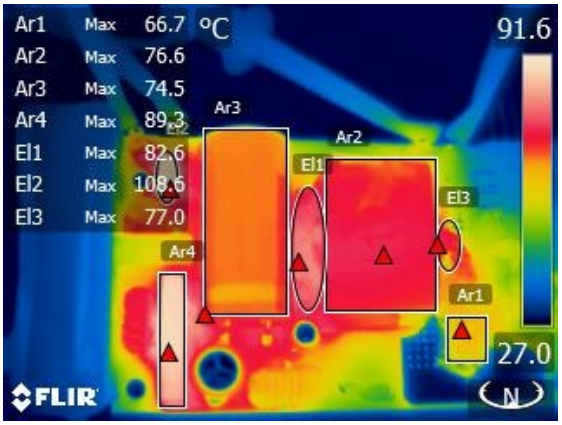


Figure 34 – Top Thermal Image.
Ar1: SR FET = 66.7 ºC.
Ar2: Transformer core, T1 = 76.6 ºC.
Ar3: Bulk Cap = 74.5 ºC.
Ar4: Bridge Rectifier = 89.3 ºC.
El1: Transformer Winding = 82.6 ºC.
El2: Thermistor, RT1= 108.6 ºC.
Ambient: = 29.2 ºC.

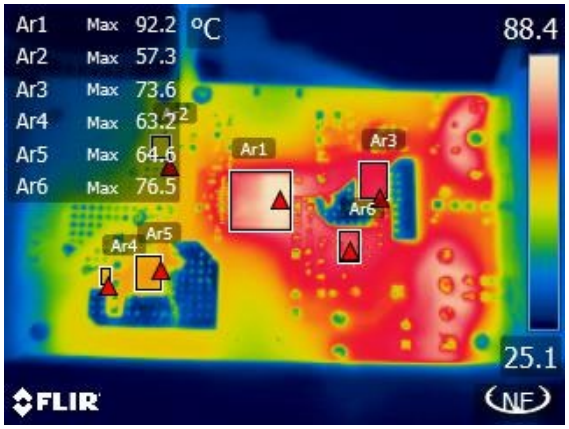


Figure 35 – Bottom Thermal Image.
Ar1: InnoSwitch4-Pro, U2 = 92.2 ºC.
Ar2: Bus Switch, Q3 = 57.3 ºC.
Ar3: Clamp Zero IC = 73.6 ºC.
Ar4: Sec. Snubber Diode = 63.2 ºC.
Ar5: Sec. Schottky Diode = 64.6 ºC.
Ar6: BJT, Q1 = 76.5 ºC.

11.8 Output: 20 V / 3 A (265 VAC)

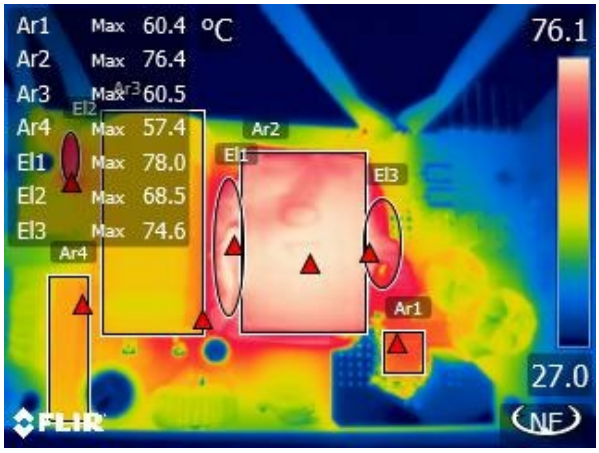


Figure 36 – Top Thermal Image.
Ar1: SR FET = 60.4 ºC.
Ar2: Transformer core, T1 = 76.4 ºC.
Ar3: Bulk Cap = 60.5 ºC.
Ar4: Bridge Rectifier = 57.4 ºC.
El1: Transformer Winding = 78 ºC.
El2: Thermistor, RT1= 68.5 ºC.
Ambient: = 29.5 ºC.

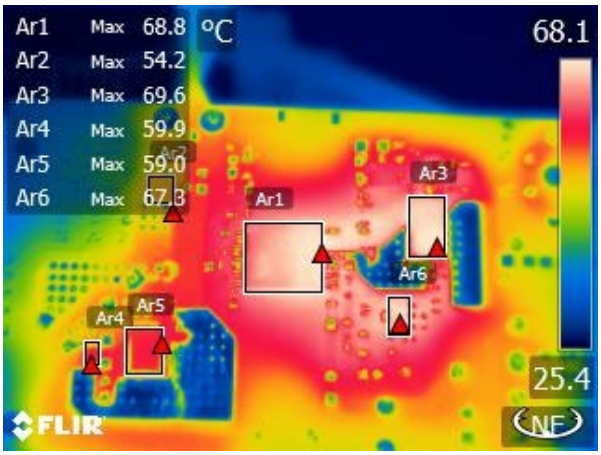


Figure 37 – Bottom Thermal Image.
Ar1: InnoSwitch4-Pro, U2 = 68.8 ºC.
Ar2: Bus Switch, Q3 = 54.2 ºC.
Ar3: Clamp Zero IC = 69.6 ºC.
Ar4: Sec. Snubber Diode = 59.9 ºC.
Ar5: Sec. Schottky Diode = 59 ºC.
Ar6: BJT, Q1 = 67.3 ºC.

12 Waveforms

12.1 Load Transient Response

Note 1: Output voltages captured on board
2: Measurements taken at room temperature

12.1.1 Output: 5 V / 3 A

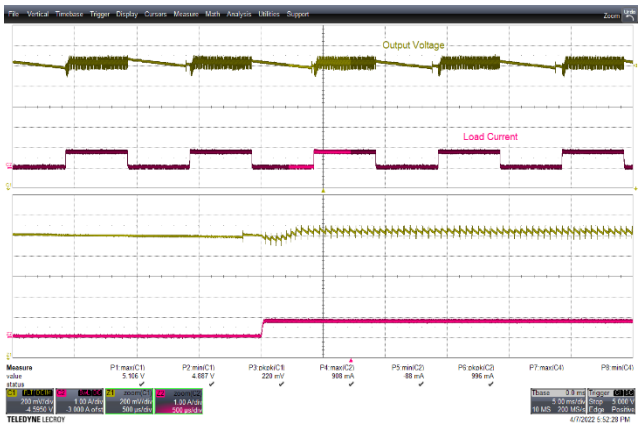


Figure 38 – Transient Response.
90 VAC, 5.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 4.887 V, V_{MAX}: 5.106 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

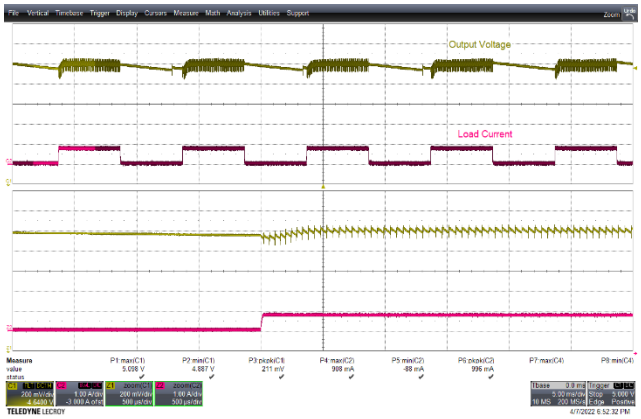


Figure 39 – Transient Response.
265 VAC, 5.0 V, 0 – 0.75 A Load Step.
V_{MIN} : 4.887 V, V_{MAX}: 5.098 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

Figure 40 – Transient Response.
90 VAC, 5.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 4.916 V, V_{MAX}: 5.171 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

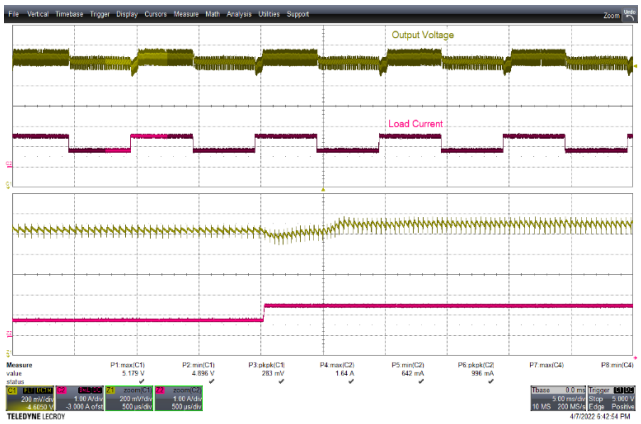


Figure 41 – Transient Response.
265 VAC, 5.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 4.896 V, V_{MAX}: 5.179 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

Figure 42 – Transient Response.
90 VAC, 5.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 4.961 V, V_{MAX}: 5.23 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

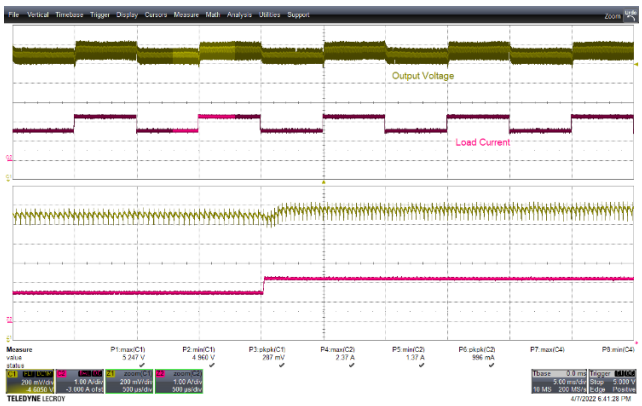


Figure 43 – Transient Response.
265 VAC, 5.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 4.96 V, V_{MAX}: 5.247 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

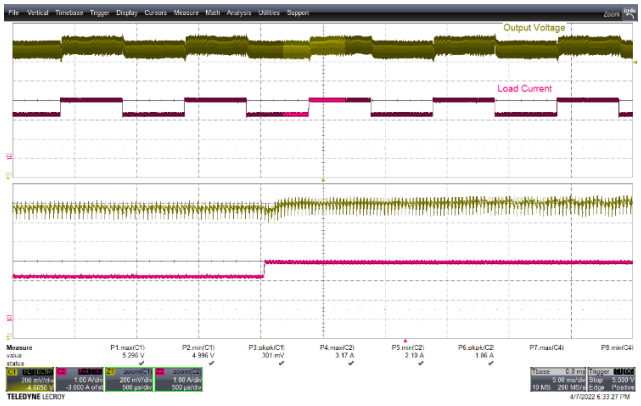


Figure 44 – Transient Response.
90 VAC, 5.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 4.996 V, V_{MAX}: 5.296 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

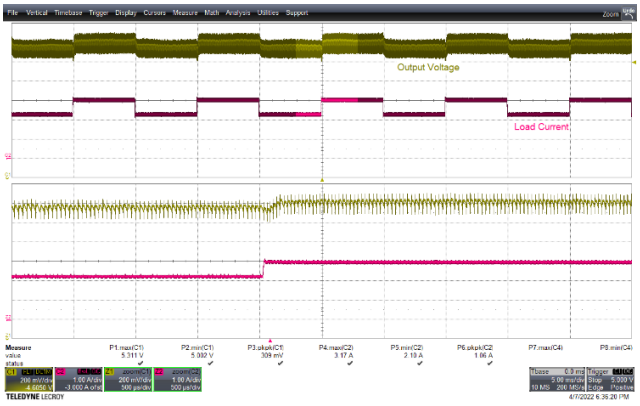


Figure 45 – Transient Response.
265 VAC, 5.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 5.002 V, V_{MAX}: 5.311 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

12.1.2 Output: 9 V / 3 A

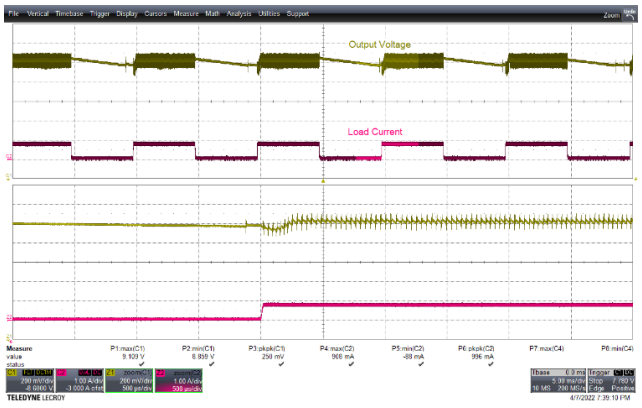


Figure 46 – Transient Response.
90 VAC, 9.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 8.859 V, V_{MAX}: 9.109 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

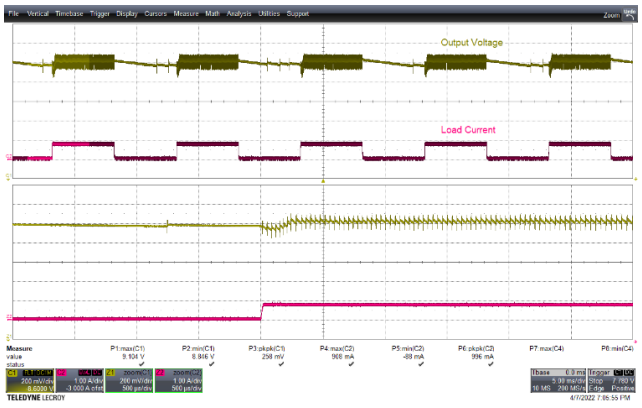


Figure 47 – Transient Response.
265 VAC, 9.0 V, 0 – 0.75 A Load Step.
V_{MIN} 8.846 V, V_{MAX}: 9.104 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

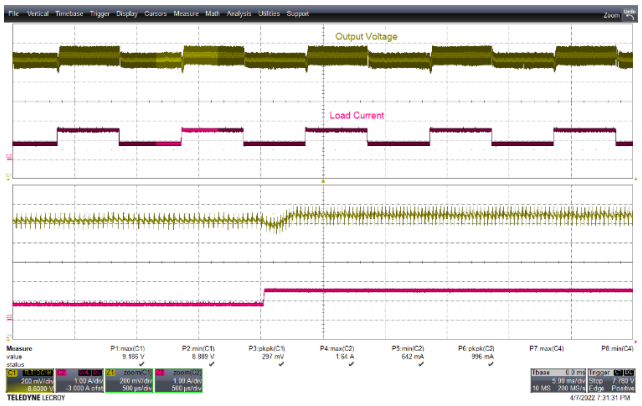


Figure 48 – Transient Response.
90 VAC, 9.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 8.889 V, V_{MAX}: 9.186 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

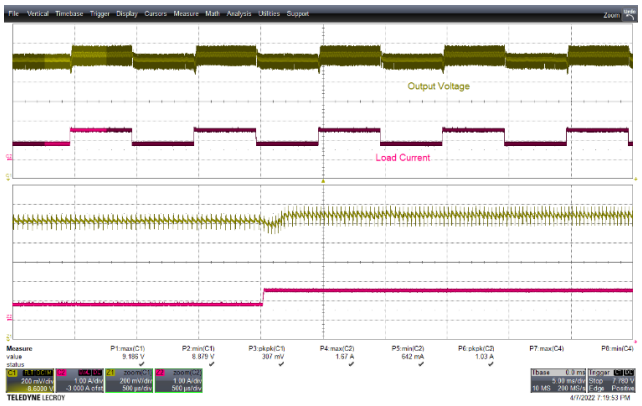


Figure 49 – Transient Response.
265 VAC, 9.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 8.879 V, V_{MAX}: 9.186 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

Figure 50 – Transient Response.
90 VAC, 9.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 8.934 V, V_{MAX}: 9.254 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

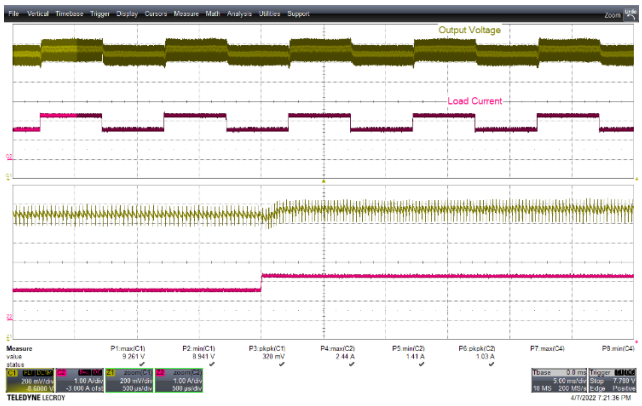


Figure 51 – Transient Response.
265 VAC, 9.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 8.941 V, V_{MAX}: 9.261 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

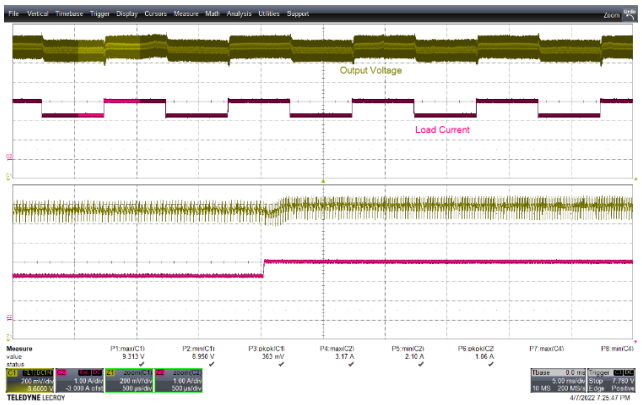


Figure 52 – Transient Response.
90 VAC, 9.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 8.95 V, V_{MAX}: 9.313 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

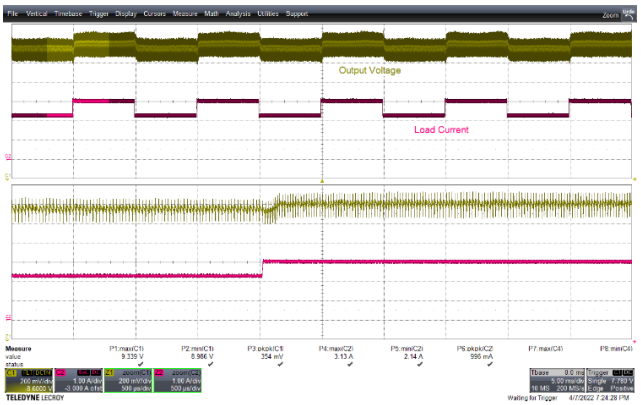


Figure 53 – Transient Response.
265 VAC, 9.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 8.986 V, V_{MAX}: 9.339 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

12.1.3 Output: 15 V / 3 A

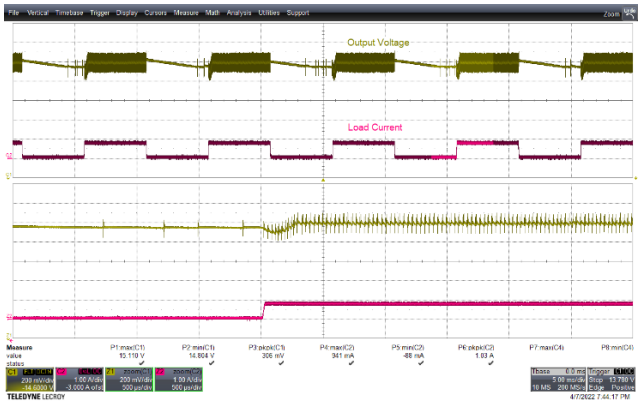


Figure 54 – Transient Response.
90 VAC, 15.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 14.804 V, V_{MAX}: 15.11 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

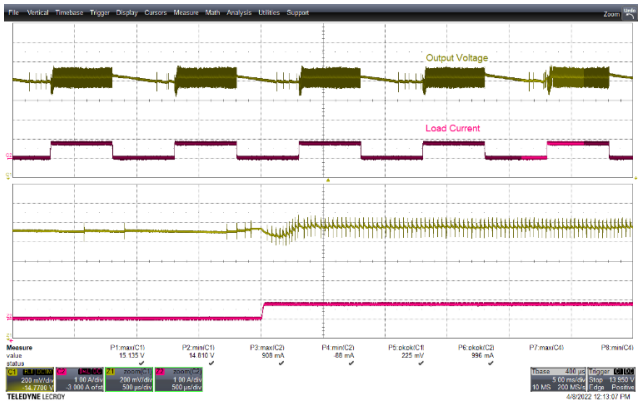


Figure 55 – Transient Response.
265 VAC, 15.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 14.810 V, V_{MAX}: 15.135 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

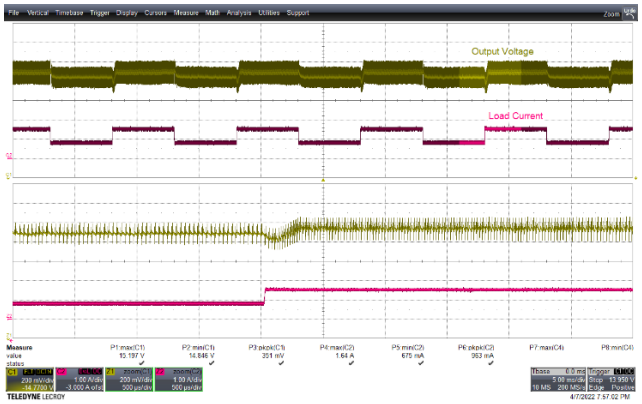


Figure 56 – Transient Response.
90 VAC, 15.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 14.846 V, V_{MAX}: 15.197 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

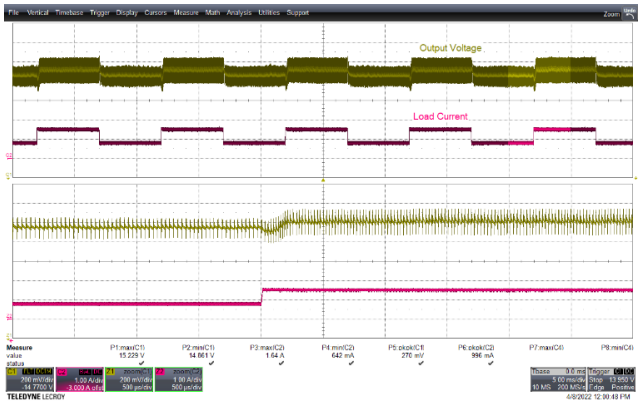


Figure 57 – Transient Response.
265 VAC, 15.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 14.861V, V_{MAX}: 15.229 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

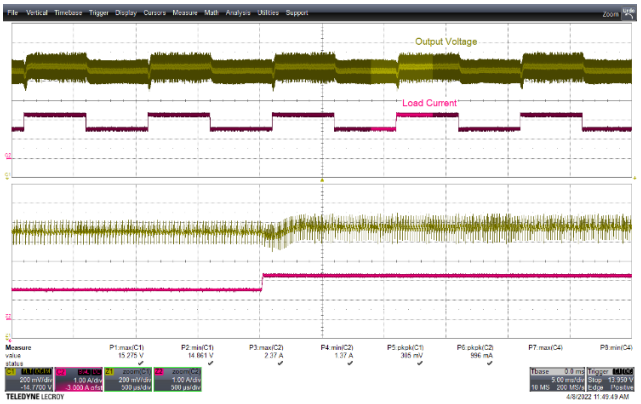


Figure 58 – Transient Response.
90 VAC, 15 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 14.861 V, V_{MAX}: 15.275 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

Figure 59 – Transient Response.
265 VAC, 15 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 14.903 V, V_{MAX}: 15.29 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

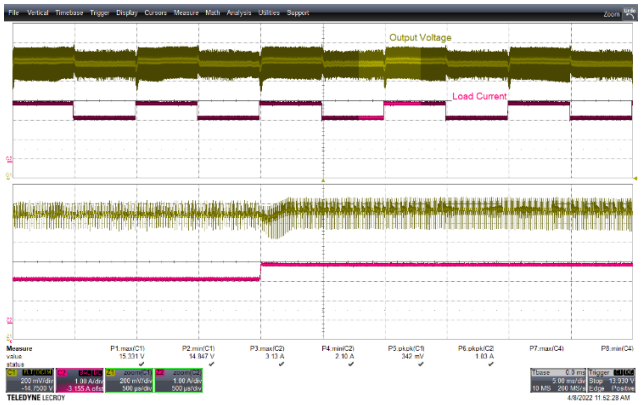


Figure 60 – Transient Response.
90 VAC, 15 V, 2.25 – 3.0 A Load Step.
V_{MIN}: 14.847V, V_{MAX}: 15.331 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

Figure 61 – Transient Response.
265 VAC, 15 V, 2.25 – 3.0 A Load Step.
V_{MIN}: 14.955 V, V_{MAX}: 15.352 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

12.1.4 Output: 20 V / 3 A

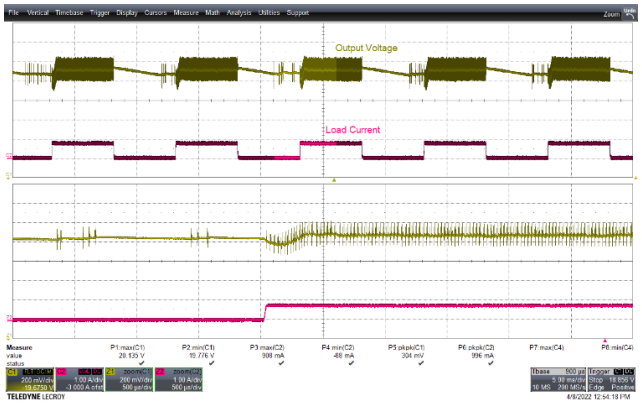


Figure 62 – Transient Response.
90 VAC, 20 V, 0 – 0.75 A Load Step.
V_{MIN}: 19.776 V, V_{MAX}: 20.135 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

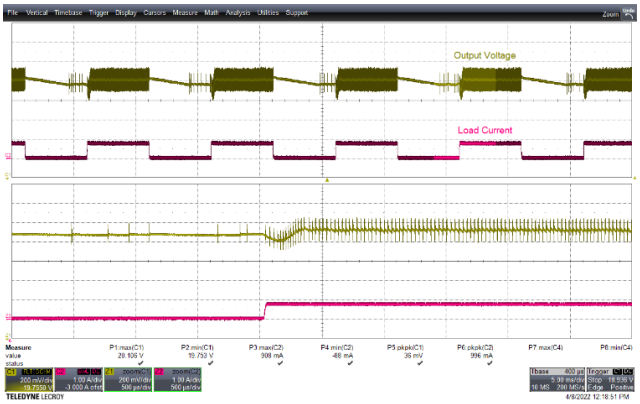


Figure 63 – Transient Response.
265 VAC, 20 V, 0 – 0.75A Load Step.
V_{MIN}: 19.753 V, V_{MAX}: 20.106 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

Figure 64 – Transient Response.
90 VAC, 20 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 19.838 V, V_{MAX}: 20.24 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

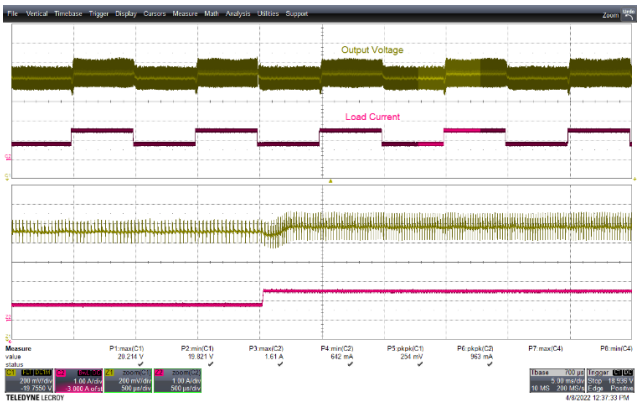


Figure 65 – Transient Response.
265 VAC, 20 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 19.821 V, V_{MAX}: 20.214 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

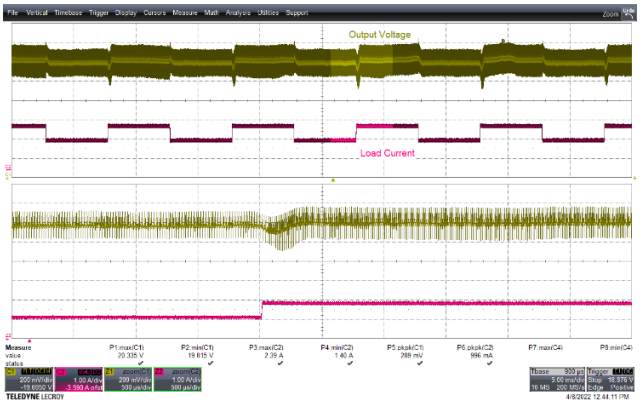


Figure 66 – Transient Response.
90 VAC, 20 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 19.815 V, V_{MAX}: 20.335 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

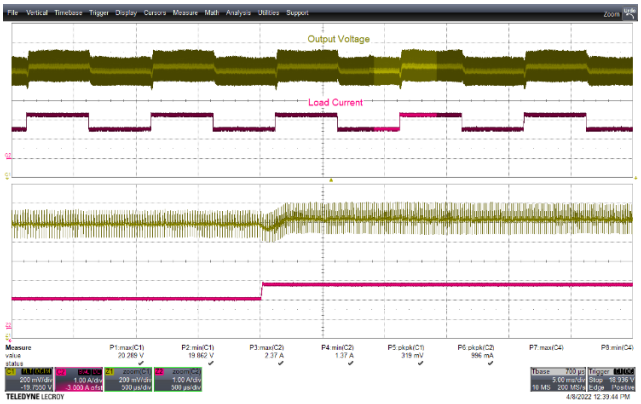


Figure 67 – Transient Response.
265 VAC, 20 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 19.862 V, V_{MAX}: 20.289 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

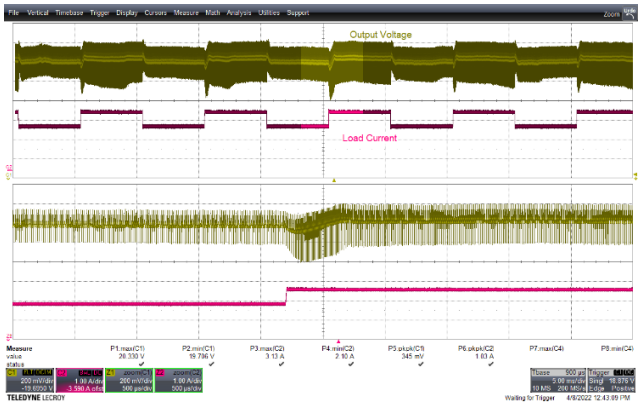


Figure 68 – Transient Response.
90 VAC, 20 V, 2.25 – 3 A Load Step.
V_{MIN}: 19.706V, V_{MAX}: 20.33 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

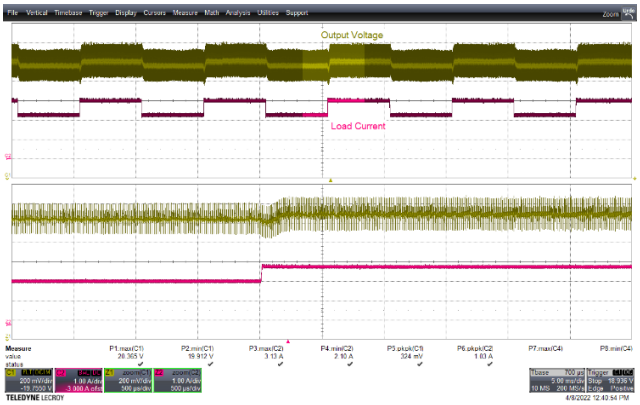


Figure 69 – Transient Response.
265 VAC, 20 V, 2.25 – 3 A Load Step.
V_{MIN}: 19.912 V, V_{MAX}: 20.365 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 0.5 ms / div.

12.2 Switching Waveforms

Note: Measurements taken at room temperature

12.2.1 Primary Drain Voltage and Current

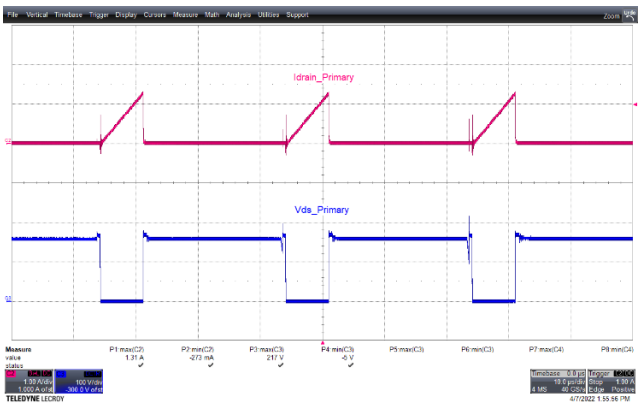


Figure 70 – Drain Voltage and Current Waveforms.
90 VAC, 5.0 V, 3 A Load (217 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 100 V / div.
Time: 10 µs / div.

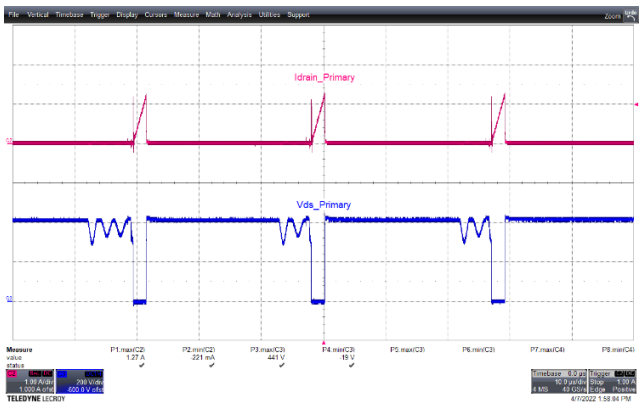


Figure 71 – Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 3 A Load (441 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 200 V / div.
Time: 10 µs / div.

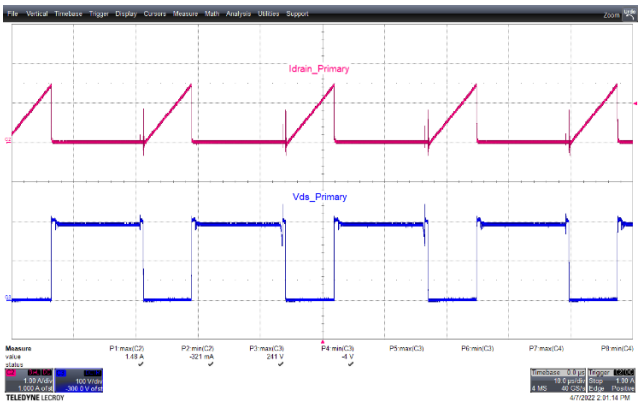


Figure 72 – Drain Voltage and Current Waveforms.
90 VAC, 9 V, 3 A Load (241 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 100 V / div.
Time: 10 µs / div.

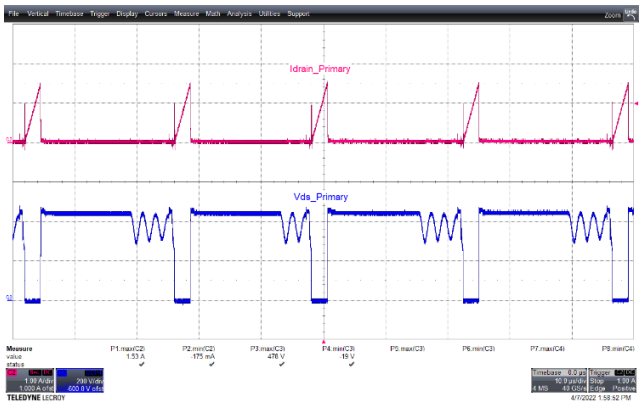


Figure 73 – Drain Voltage and Current Waveforms.
265 VAC, 9 V, 3 A Load (478 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 200 V / div.
Time: 10 µs / div.

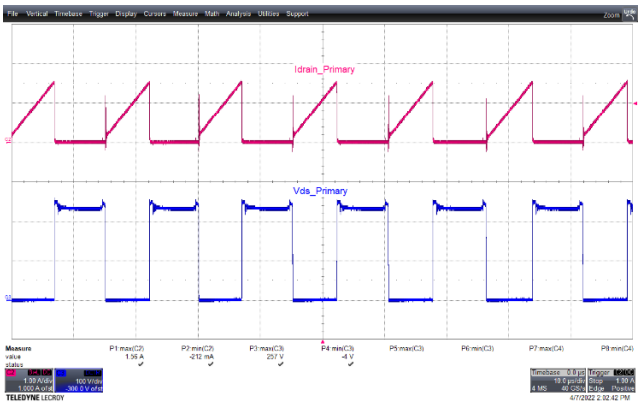


Figure 74 – Drain Voltage and Current Waveforms.
90 VAC, 15.0 V, 3 A Load (257 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 100 V / div.
Time: 10 μs / div.

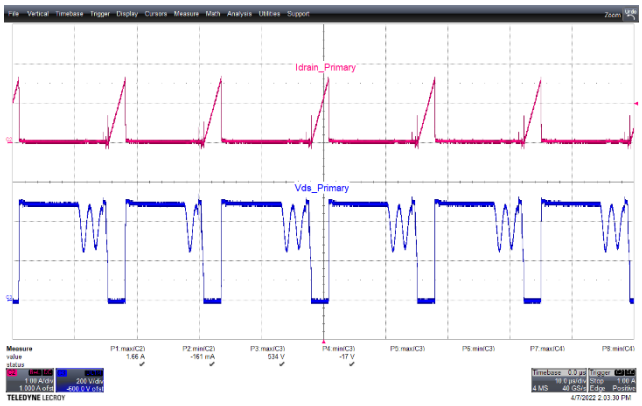


Figure 75 – Drain Voltage and Current Waveforms.
265 VAC, 15.0 V, 3 A Load (534 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 200 V / div.
Time: 10 μs / div..

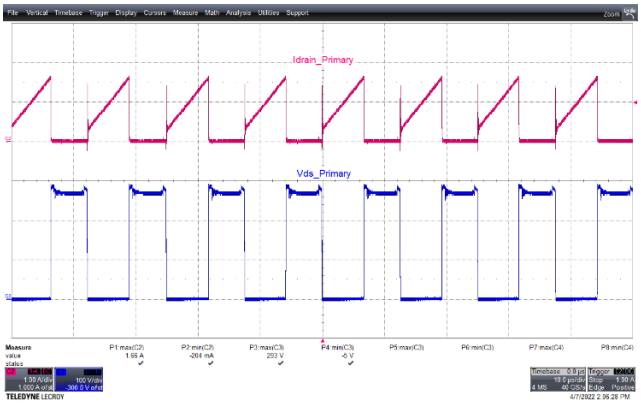


Figure 76 – Drain Voltage and Current Waveforms.
90 VAC, 20 V, 3 A Load (293 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 100 V / div.
Time: 10 μs / div.

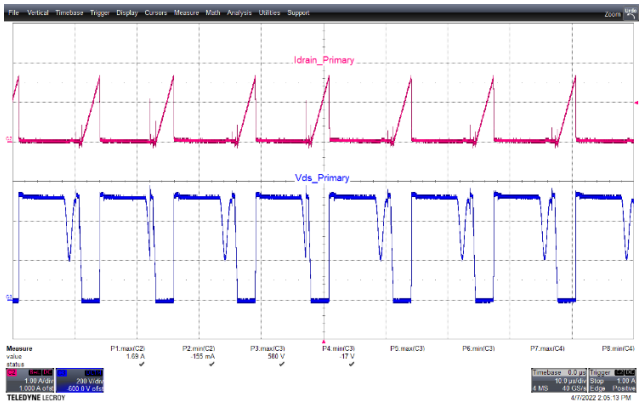


Figure 77 – Drain Voltage and Current Waveforms.
265 VAC, 20 V, 3 A Load (580 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 200 V / div.
Time: 10 μs / div.

12.2.2 SR FET Voltage

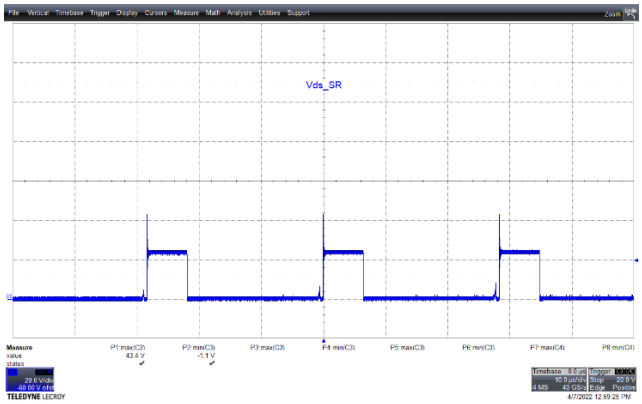


Figure 78 – SR FET Voltage Waveforms.
90 VAC, 5.0 V, 3 A Load (43.4 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 10 μs / div.

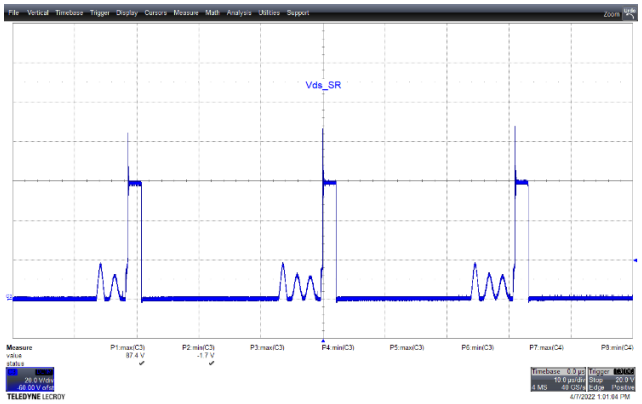


Figure 79 – SR FET Voltage Waveforms.
265 VAC, 5.0 V, 3 A Load (87.4 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 10 μs / div.

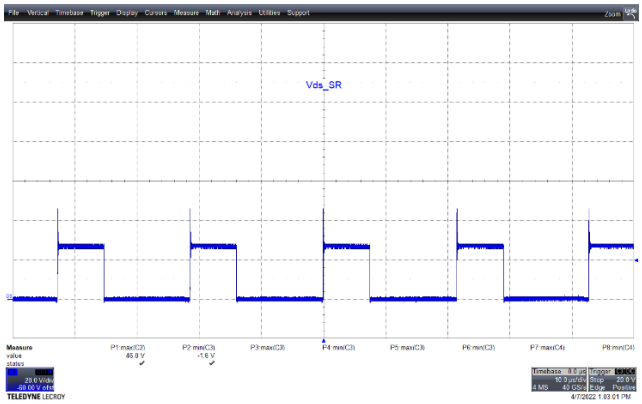


Figure 80 – SR FET Voltage Waveforms.
90 VAC, 9.0 V, 3 A Load (46.0 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 10 μs / div.

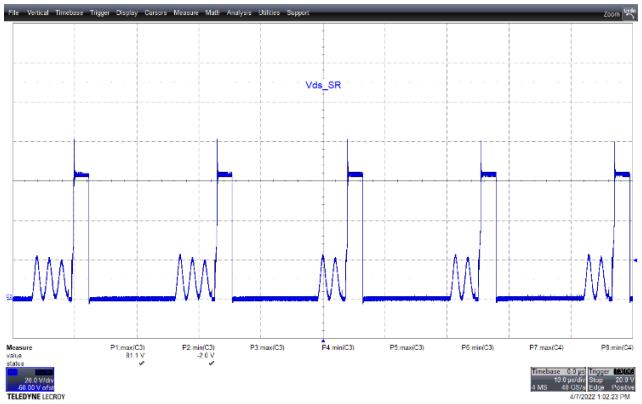


Figure 81 – SR FET Voltage Waveforms.
265 VAC, 9.0 V, 3 A Load (81.1 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 10 μs / div.

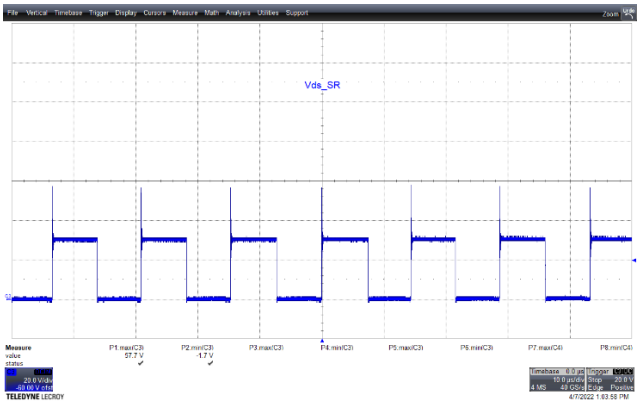


Figure 82 – SR FET Voltage Waveforms.
90 VAC, 15.0 V, 3 A Load (57.7 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 10 μs / div.

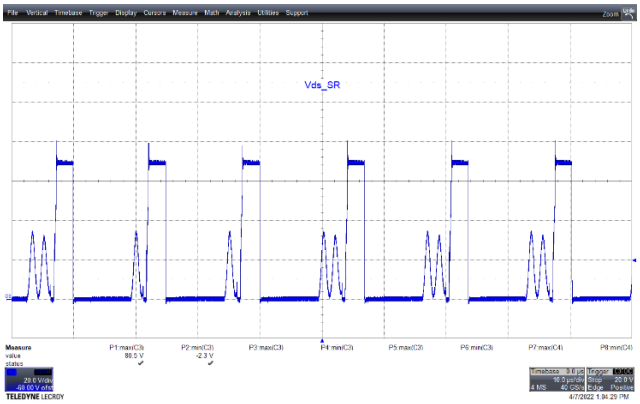


Figure 83 – SR FET Voltage Waveforms.
265 VAC, 15.0 V,3 A Load (80.5 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 10 μs / div.

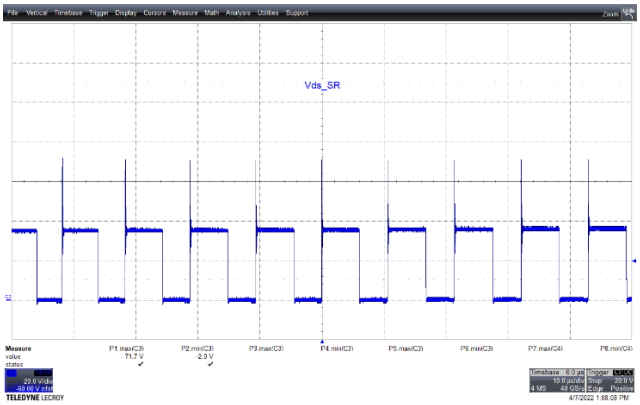


Figure 84 – SR FET Voltage Waveforms.
90 VAC, 20 V, 3 A Load (71.7 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 10 μs / div.

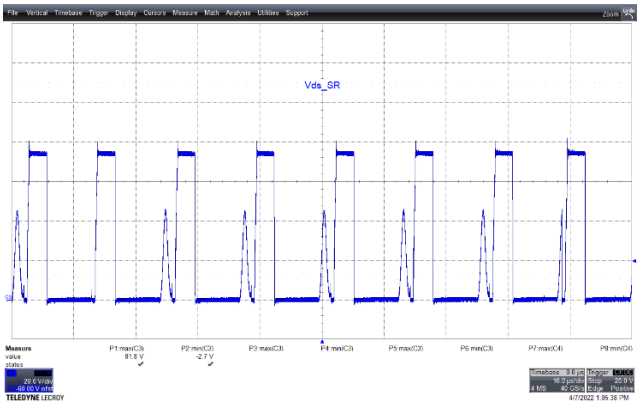


Figure 85 – SR FET Voltage Waveforms.
265 VAC, 20 V, 3 A Load (81.8 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 10 μs / div.

12.3 Start-up

Note: Measurements taken at room temperature

12.3.1 Primary FET

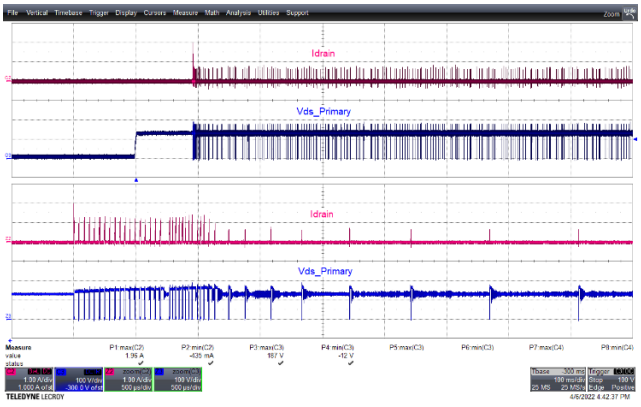


Figure 86 – Drain Voltage and Current Waveforms.
90 VAC, 5.0 V, 0 A Load (187 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 100 V / div.
Time: 100 ms / div.
(Zoom: 500 µs / div.)

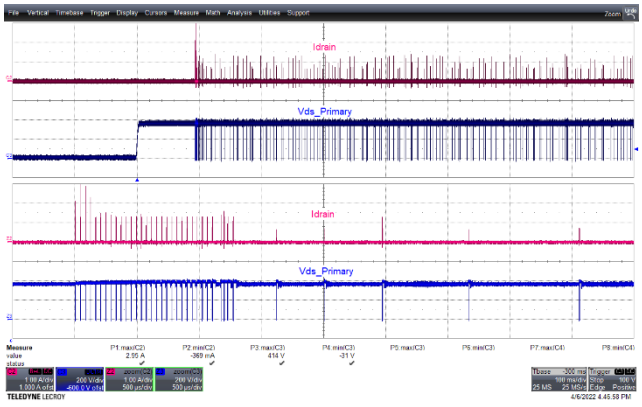


Figure 87 – Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 0 A Load (414 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 200 V / div.
Time: 100 ms / div.
(Zoom: 500 µs / div.)

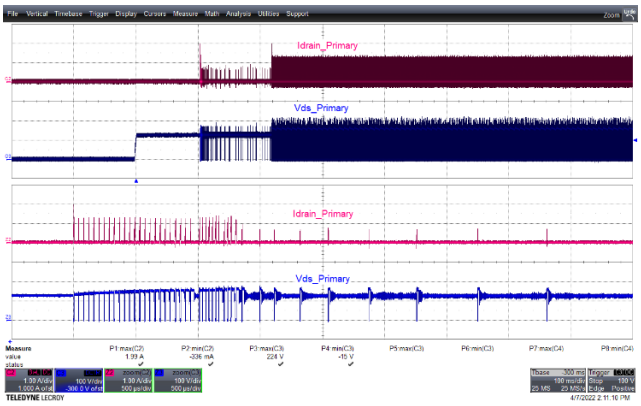


Figure 88 – Drain Voltage and Current Waveforms.
90 VAC, 5.0 V, 3 A Load (224 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 100 V / div.
Time: 100 ms / div.
(Zoom: 500 µs / div.)

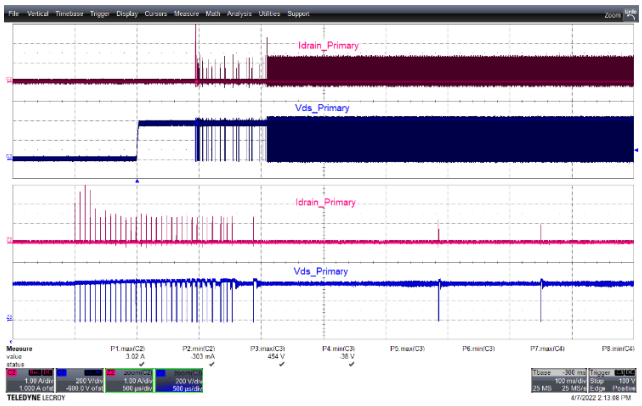


Figure 89 – Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 3 A Load (454 V_{MAX}).
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 200 V / div.
Time: 100 ms / div.
(Zoom: 500 µs / div.)

12.3.2 SR FET

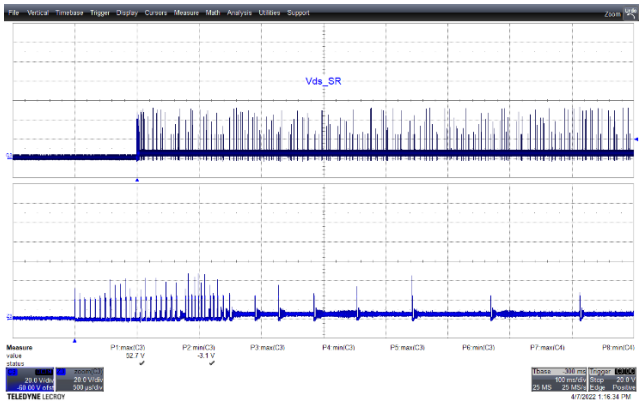


Figure 90 – SR FET Voltage Waveforms.
90 VAC, 5.0 V, 0 A Load (52.7 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 100 ms / div. (Zoom: 500 μs / div.)

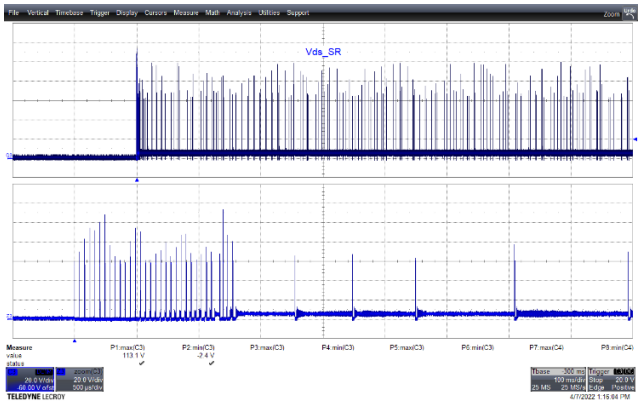


Figure 91 – SR FET Voltage Waveforms.
265 VAC, 5.0 V, 0 A Load (113.1 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 100 ms / div. (Zoom: 500 μs / div.)

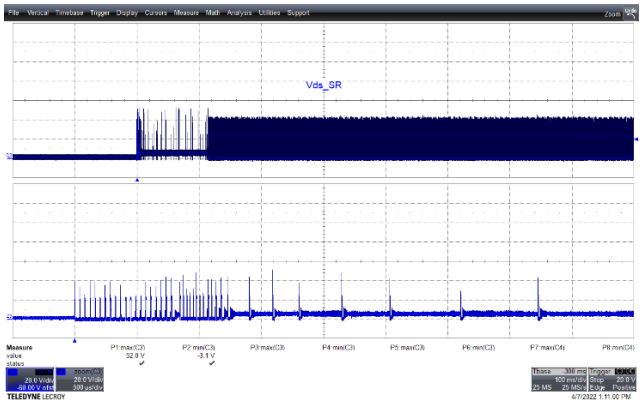


Figure 92 – SR FET Voltage Waveforms.
90 VAC, 5.0 V, 3 A Load (52 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 100 ms / div. (Zoom: 500 μs / div.)

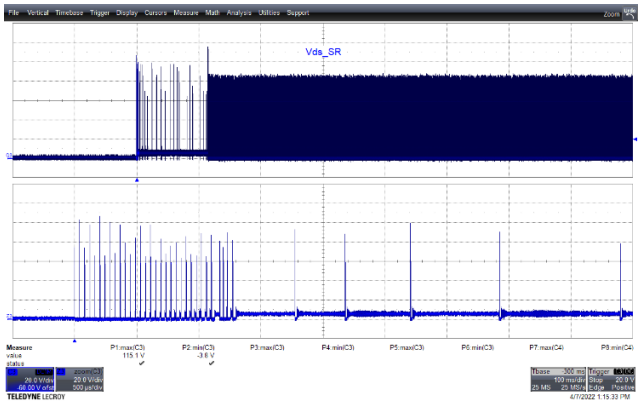


Figure 93 – SR FET Voltage Waveforms.
265 VAC, 5.0 V, 3 A Load (115.1 V_{MAX}).
Scale: V_{DRAIN}, 20 V / div.
Time: 100 ms / div. (Zoom: 500 μs / div.)

13 Output Ripple Measurements

13.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

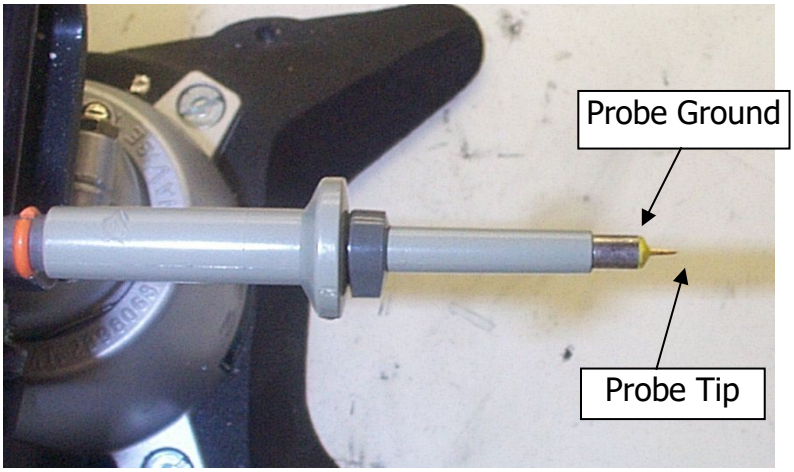


Figure 94 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

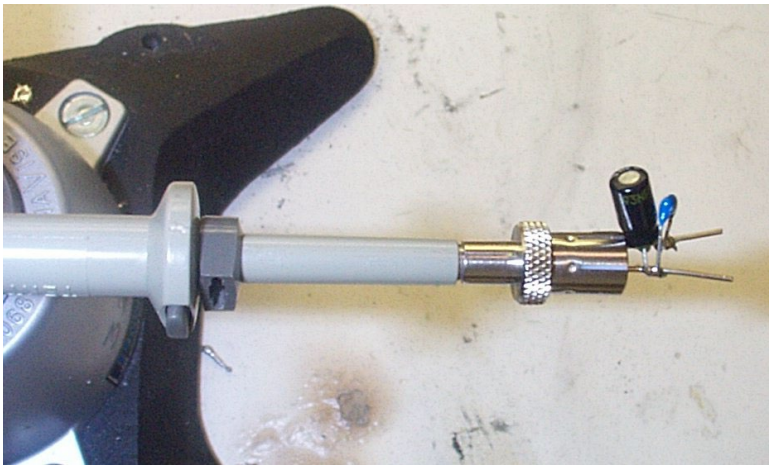


Figure 95 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.2 Output Voltage Ripple Waveforms

Note 1: Output voltages captured at the end of 100mΩ cable
2: Measurements taken at room temperature

13.2.1 Output: 5 V / 3 A

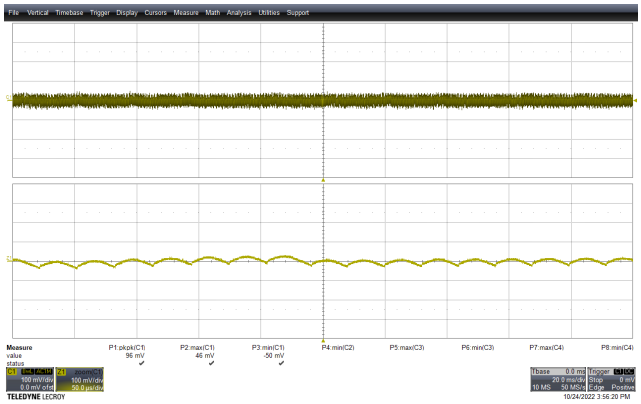


Figure 96 – Output Ripple. PK-PK = 96 mV.
90 VAC_{IN} 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 μs / div.

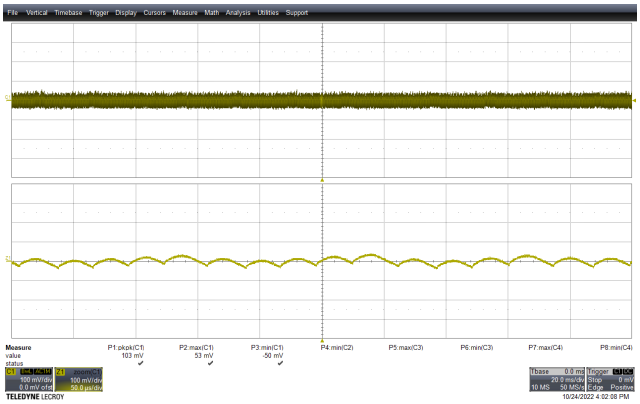


Figure 97 – Output Ripple. PK-PK = 103 mV.
115 VAC_{IN} 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 μs / div.

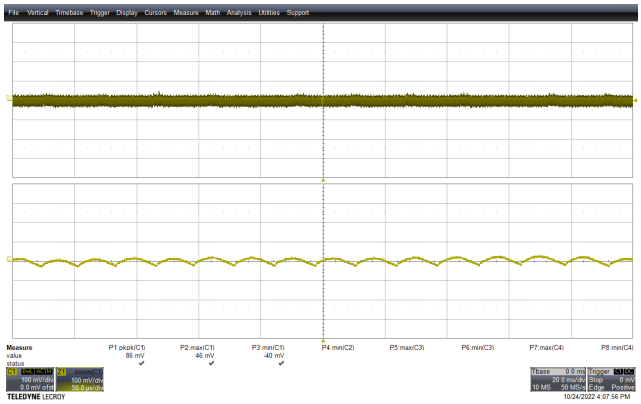


Figure 98 – Output Ripple. PK-PK = 86 mV.
230 VAC_{IN} 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 μs / div.

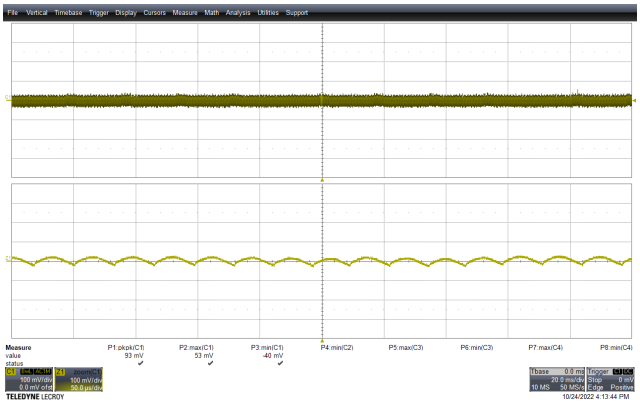


Figure 99 – Output Ripple. PK-PK = 93 mV.
265 VAC_{IN} 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 μs / div.

13.2.2 Output: 9 V / 3 A

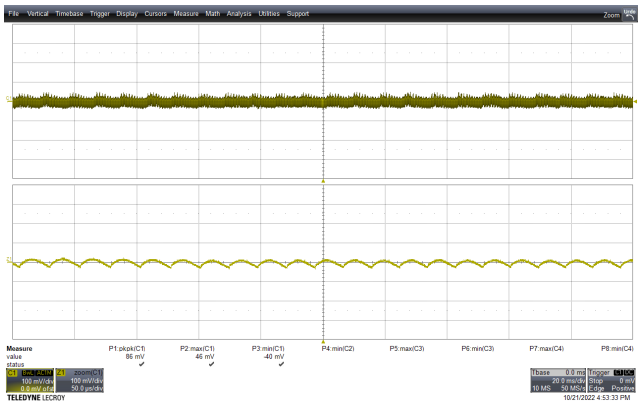


Figure 100 – Output Ripple. PK-PK = 86 mV
90 VAC_{IN} 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

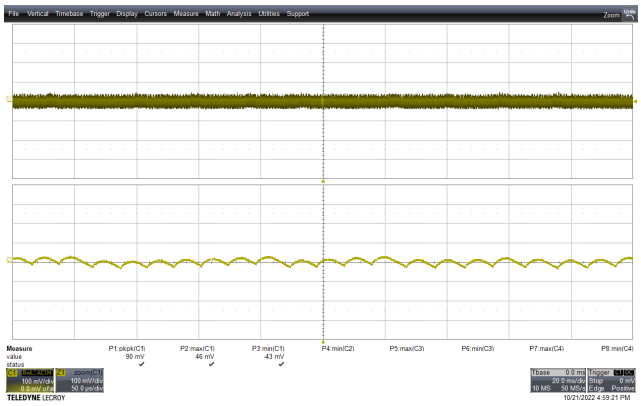


Figure 101 – Output Ripple. PK-PK = 90 mV
115 VAC_{IN} 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

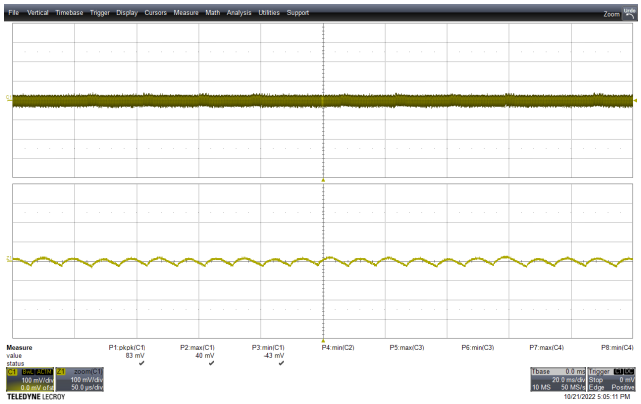


Figure 102 – Output Ripple. PK-PK = 83 mV
230 VAC_{IN} 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

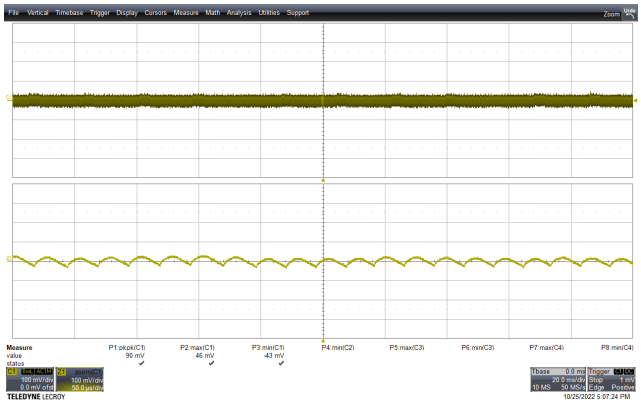


Figure 103 – Output Ripple. PK-PK = 90 mV
265 VAC_{IN} 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

13.2.3 Output: 15 V / 3 A

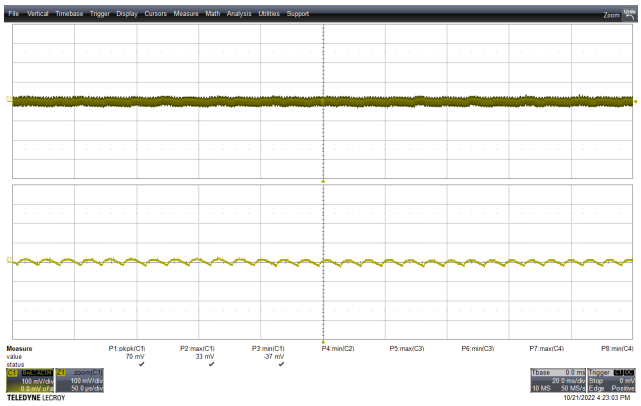


Figure 104 – Output Ripple. PK-PK = 70 mV.
90 VAC_{IN}, 15.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 μs / div.

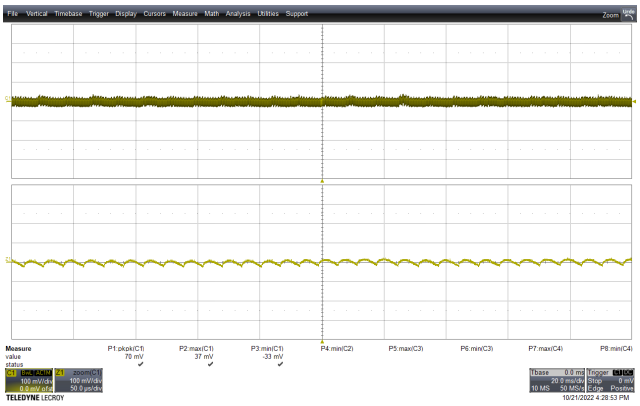


Figure 105 – Output Ripple. PK-PK = 70 mV.
115 VAC_{IN} 15.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 μs / div.

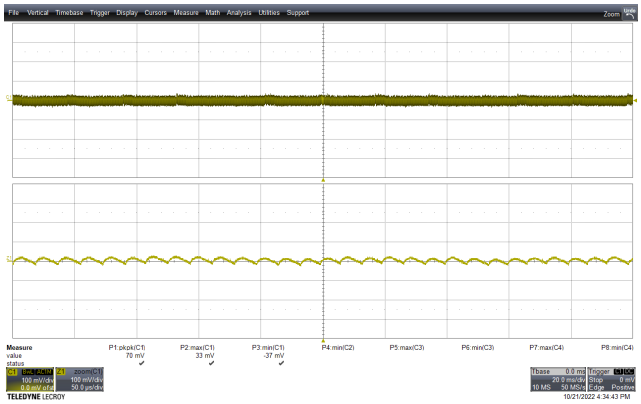


Figure 106 – Output Ripple. PK-PK = 70 mV.
230 VAC_{IN} 15.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 μs / div.

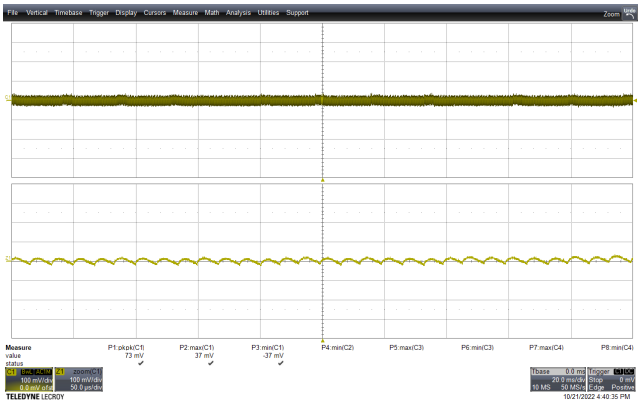


Figure 107 – Output Ripple. PK-PK = 73 mV.
265 VAC_{IN} 15.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 μs / div.

13.2.4 Output: 20 V / 3 A

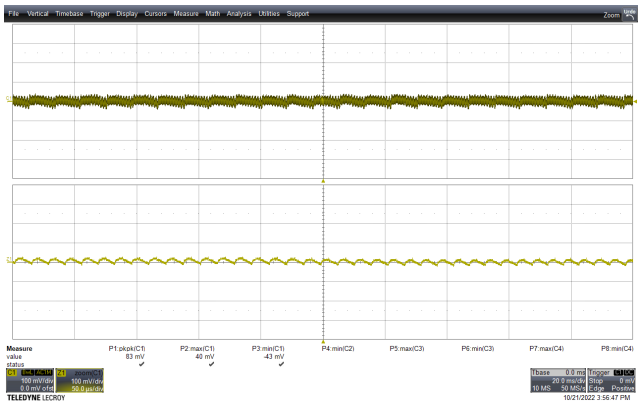


Figure 108 – Output Ripple. PK-PK = 83 mV.
90 VAC_{IN}, 20 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

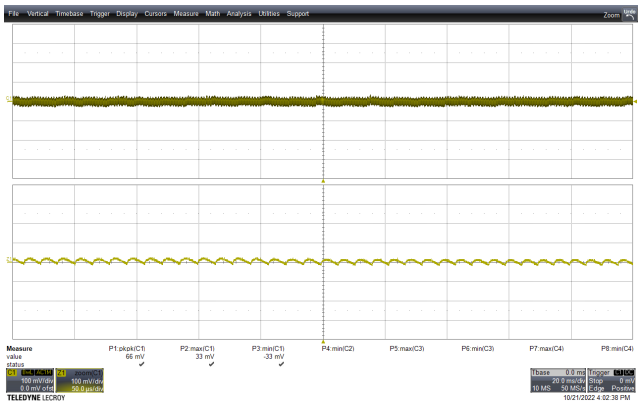


Figure 109 – Output Ripple. PK-PK = 66 mV.
115 VAC_{IN}, 20 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

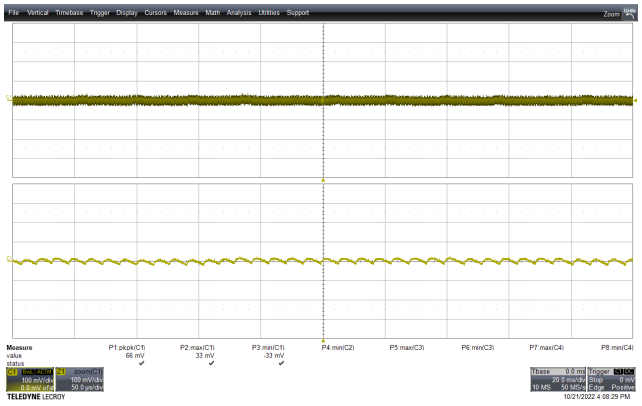


Figure 110 – Output Ripple. PK-PK = 66 mV.
230 VAC_{IN} 20 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

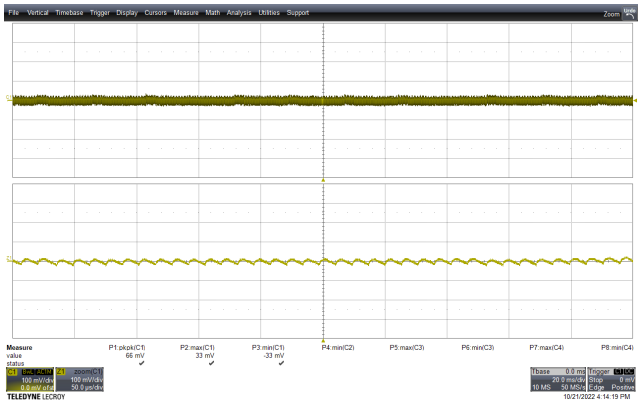


Figure 111 – Output Ripple. PK-PK = 66 mV.
265 VAC_{IN} 20 V, 3 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

13.3 Output Voltage Ripple Amplitude

Note 1: Output voltages captured at the end of 100mΩ cable
2: Measurements taken at room temperature

13.3.1 Output: 5 V / 3 A

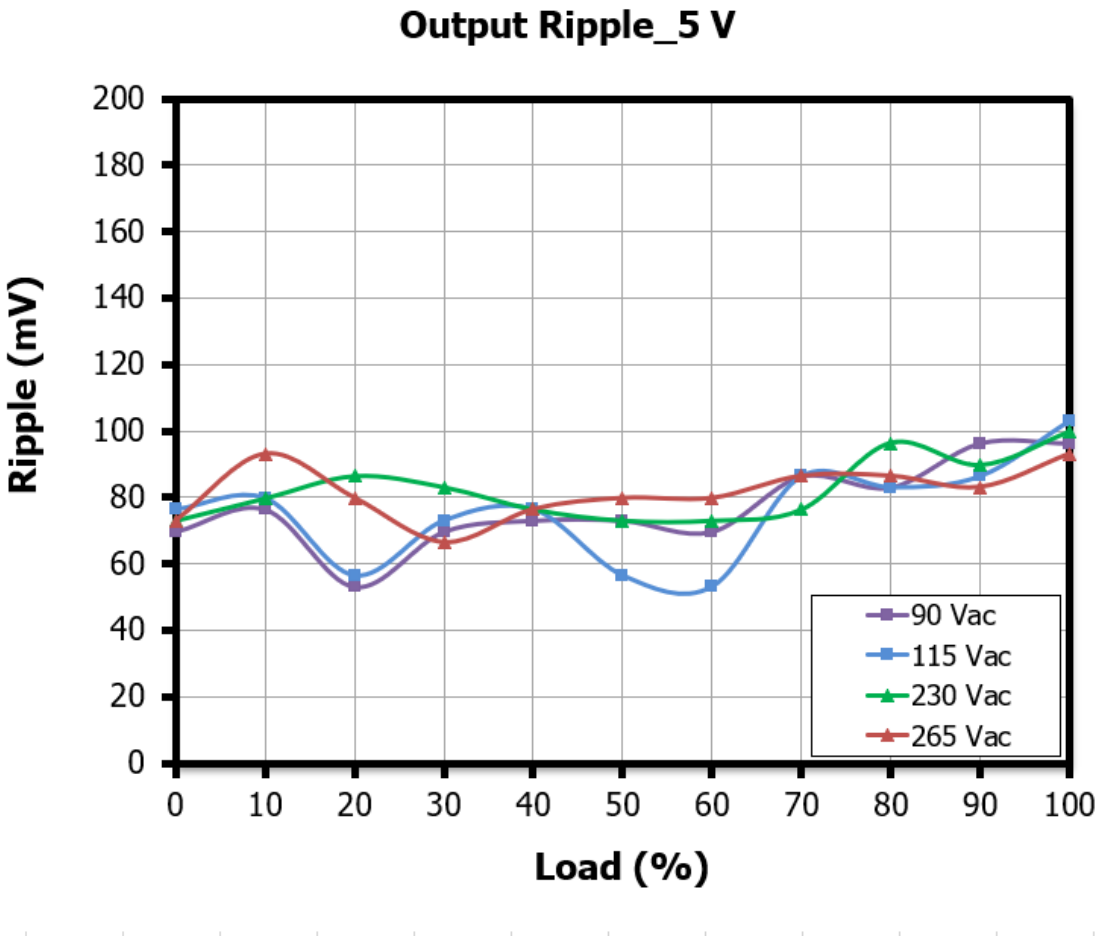


Figure 112 – 5 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.2 Output: 9 V / 3 A

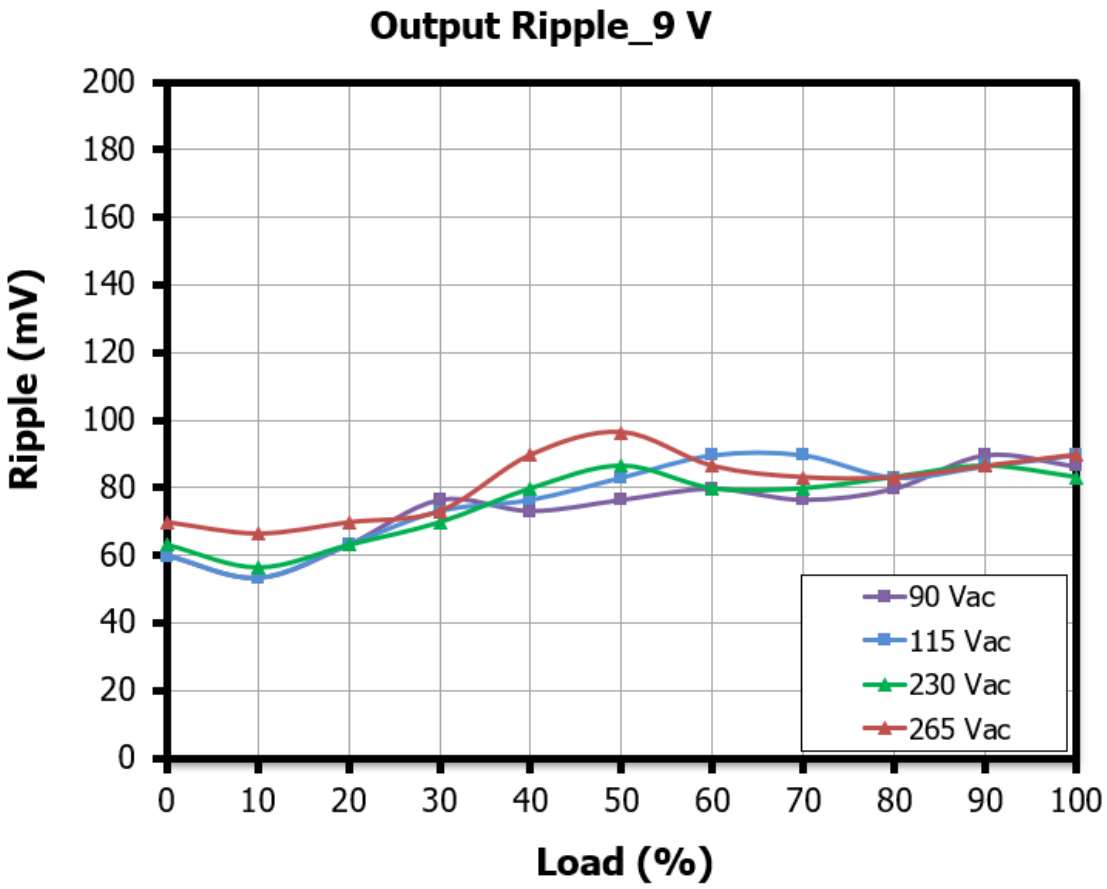


Figure 113 – 9 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.3 Output: 15 V / 3 A

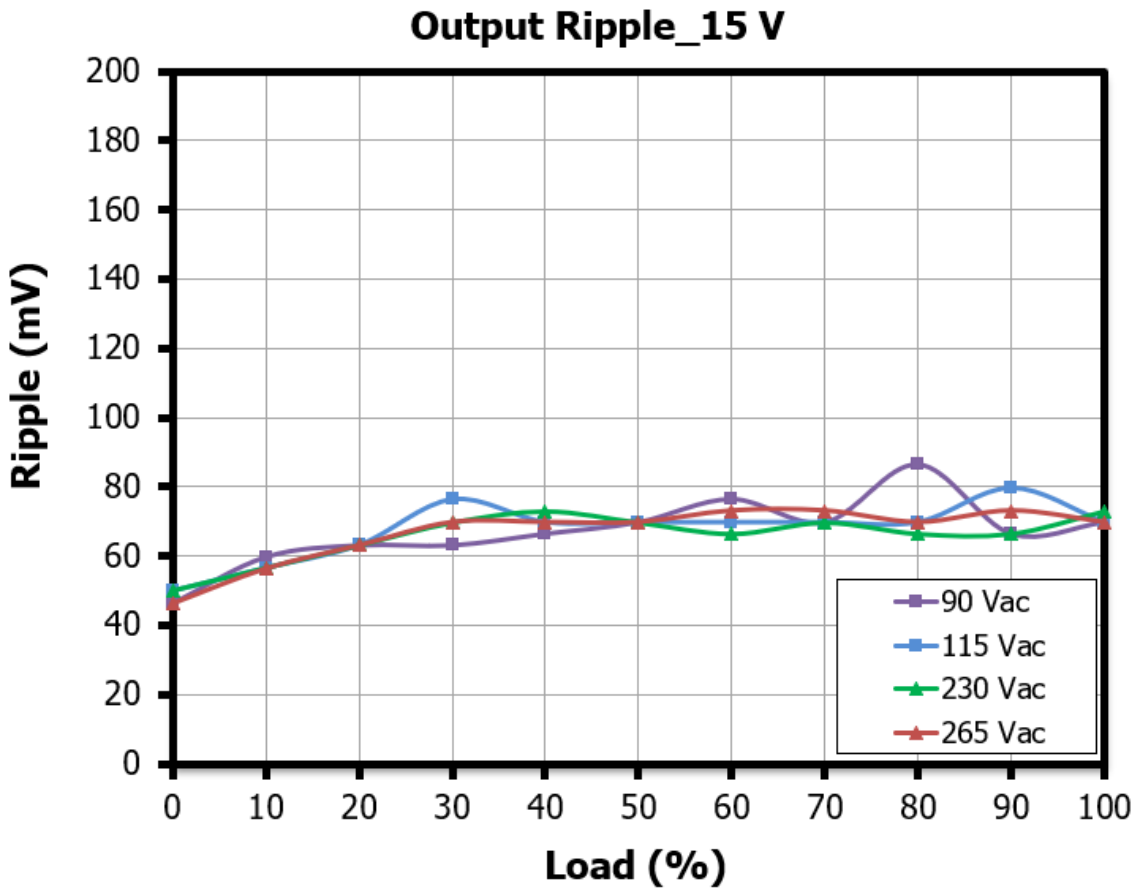


Figure 114 – 15 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.4 Output: 20 V / 3 A

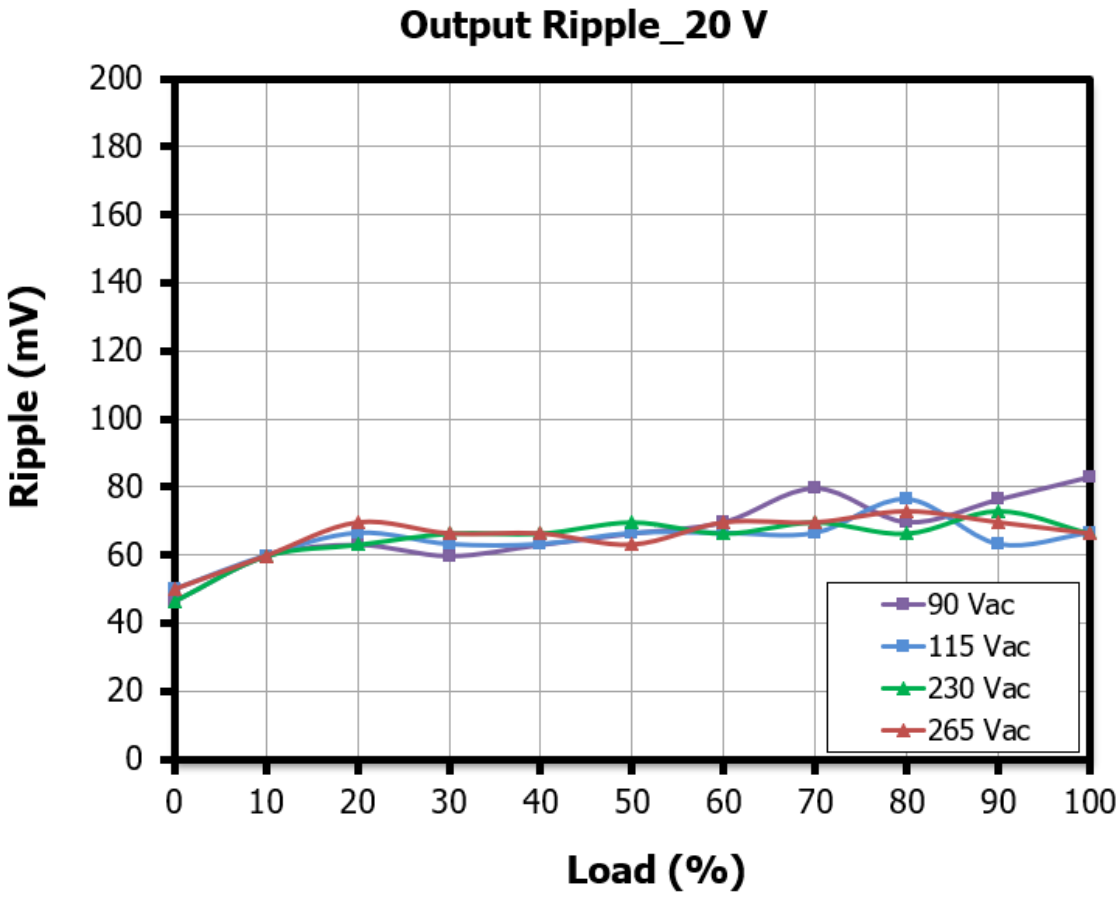


Figure 115 – 20 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

14 CV/CC Profile

CVCC profiles were taken with the output voltage measured on the board at room temperature. The PIC microcontroller is configured such that the constant current limit of InnoSwitch4-Pro is set above the rated output current 3 A by +150 mA i.e. constant current limit is set to 3.15 A.

NOTE: Positive slope of output voltage vs. load in CV region in all figures below is due to CDC used (300 mV)

14.1 Output: 20 V / 3 A

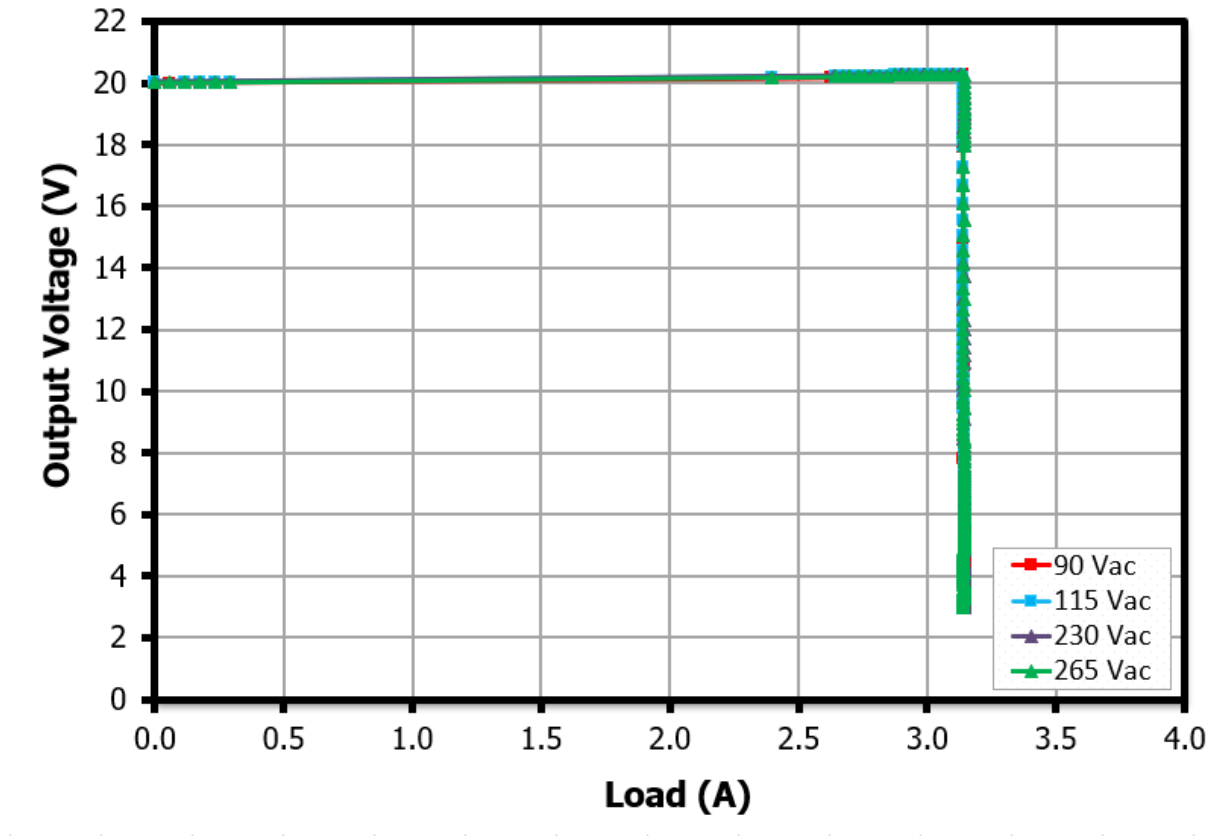


Figure 116 – CV/CC Profile with Output 20 V, 3 A.

14.2 Output: 15 V / 3 A

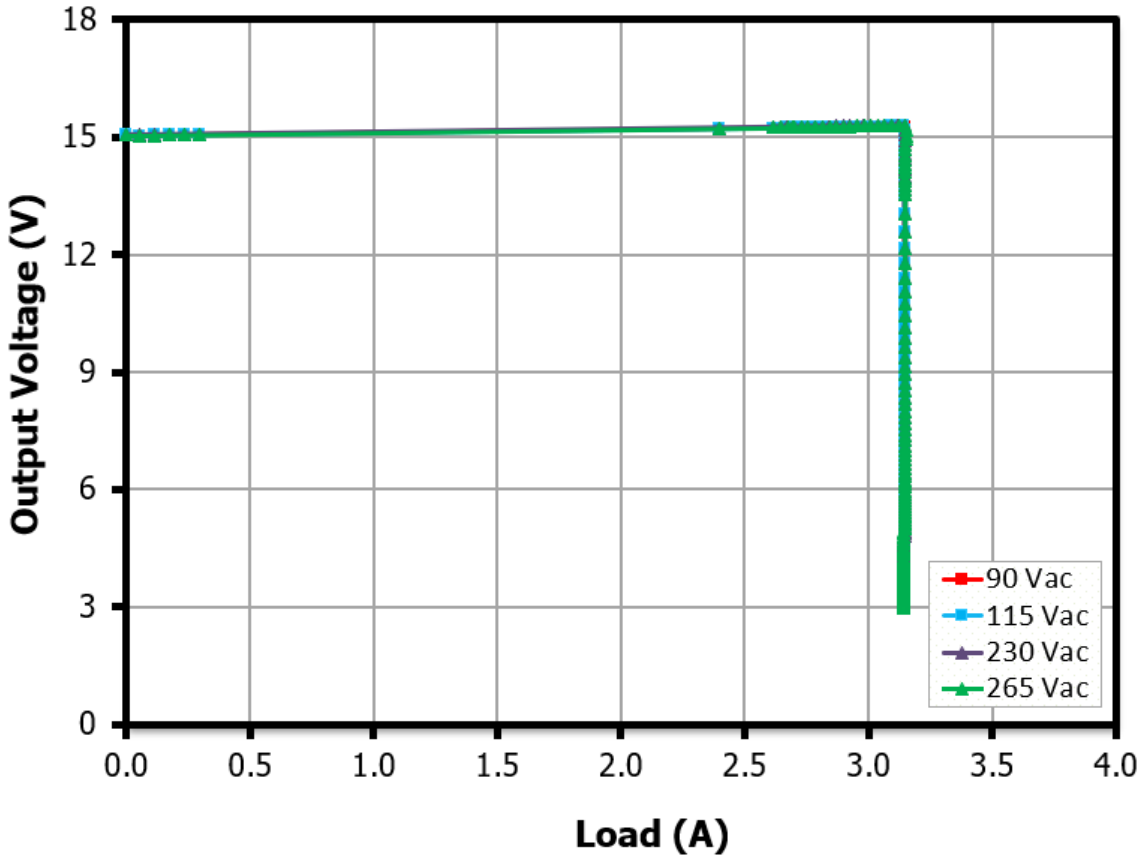


Figure 117 – CV/CC Profile with Output 15 V, 3 A.

14.3 Output: 9 V / 3 A

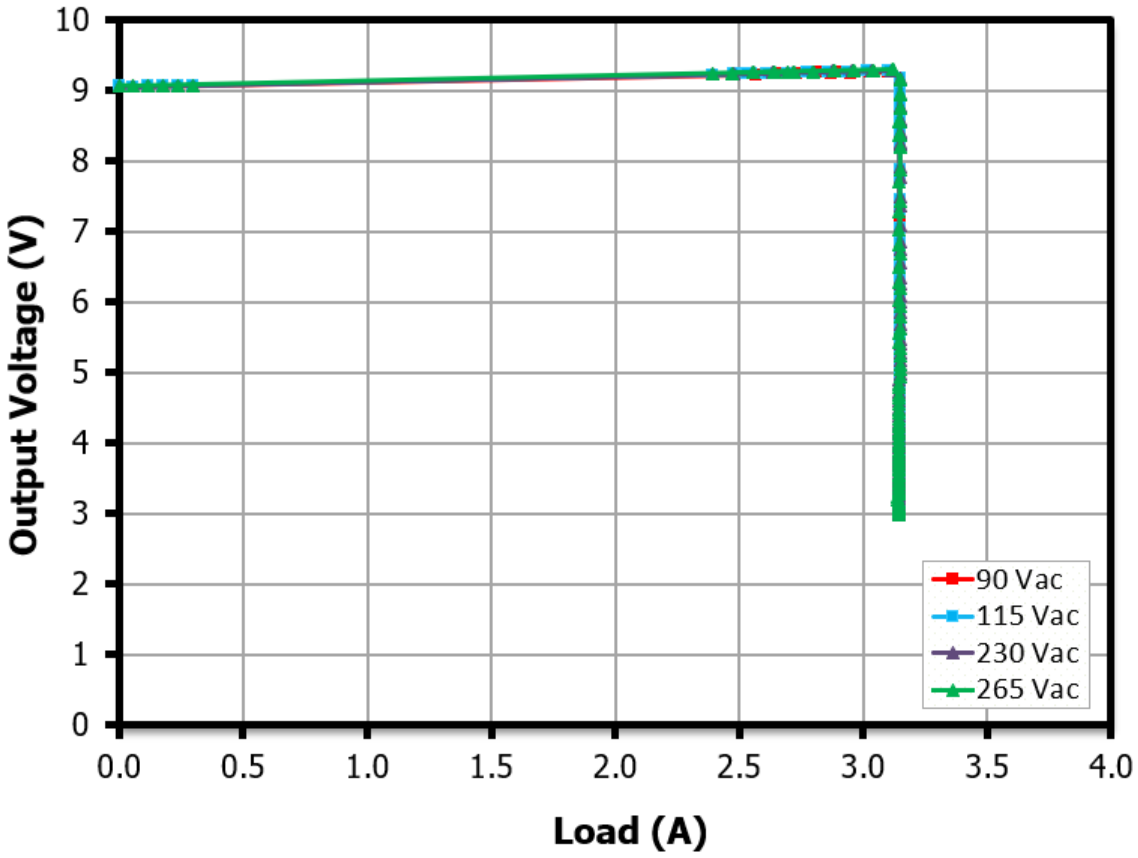


Figure 118 – CV/CC Profile with Output 9 V, 3 A.

14.4 Output: 5 V / 3 A

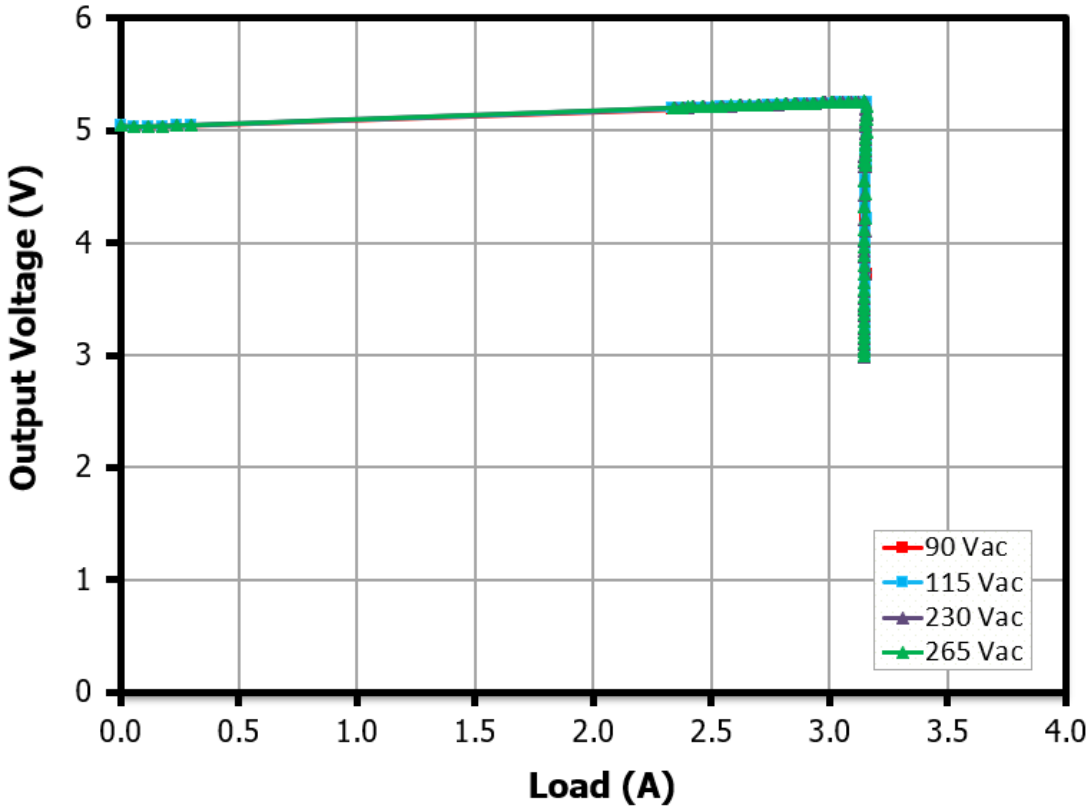
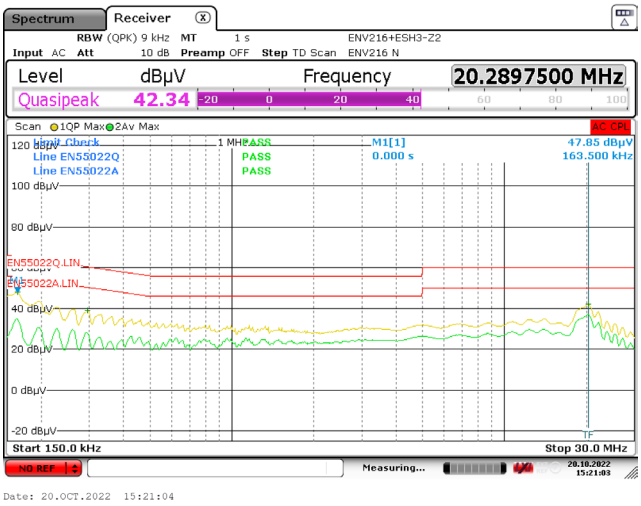


Figure 119 – CV/CC Profile with Output 5 V, 3 A.

15 Conducted EMI

15.1 Earth Floating (QPK / AV)

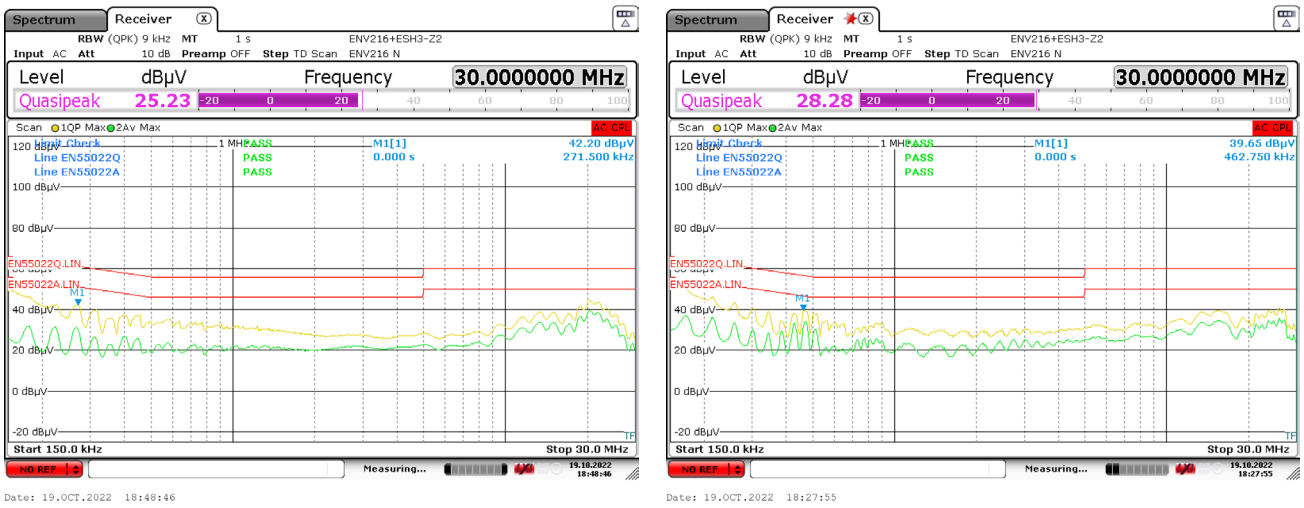
15.1.1 Output: 5 V / 3 A



115 VAC$_{IN}$. 230 VAC$_{IN}$.

Figure 120 –Floating Ground EMI, 5 V / 3 A Load.

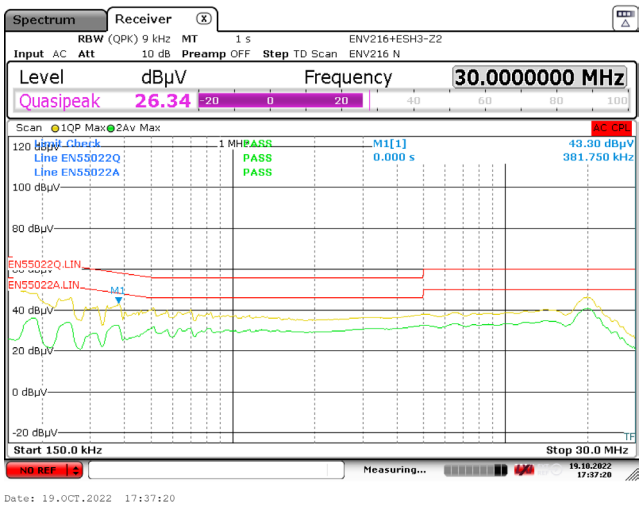
15.1.2 Output: 9 V / 3 A



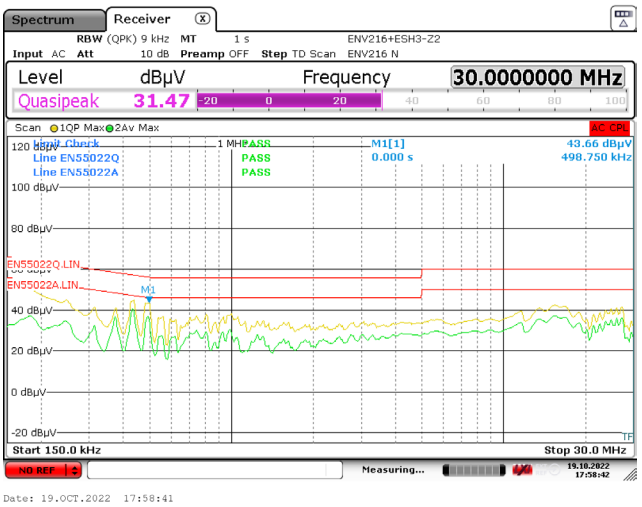
115 VAC$_{IN}$. 230 VAC$_{IN}$.

Figure 121 – Floating Ground EMI, 9 V / 3 A Load.

15.1.3 Output: 15 V / 3 A



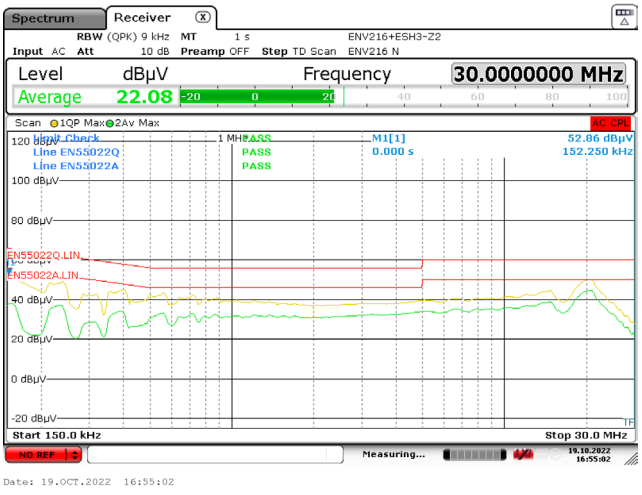
115 VAC_{IN}.



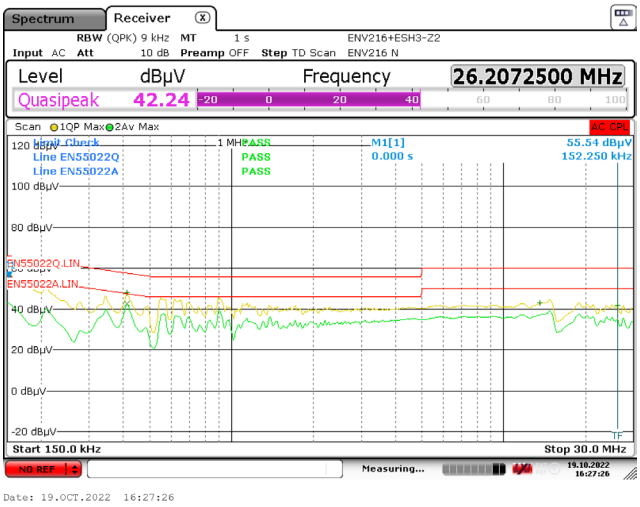
230 VAC_{IN}.

Figure 122 – Floating Ground EMI, 15 V / 3 A Load.

15.1.4 Output: 20 V / 3 A



115 VAC_{IN}.



230 VAC_{IN}.

Figure 123 – Floating Ground EMI, 20 V / 3 A Load.

16 Combination Wave Surge

The unit was subjected to ±1500 V differential mode and ±3000 V common mode combination wave and ring wave surge at several line phase angles with 10 strikes for each condition. Note that AR might be observed due to line OV/UV protection mechanism triggered during the test, which is a normal protection feature of the InnoSwitch4-Pro - CZ IC.

16.1 Differential Mode Surge (L1 to L2), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 3 A (Pass / Fail)
+1500	L1 to L2	0	Pass
-1500	L1 to L2	0	Pass
+1500	L1 to L2	90	Pass
-1500	L1 to L2	90	Pass
+1500	L1 to L2	180	Pass
-1500	L1 to L2	180	Pass
+1500	L1 to L2	270	Pass
-1500	L1 to L2	270	Pass

16.2 Common Mode Surge (L1 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 3 A (Pass / Fail)
+3000	L1 to PE	0	Pass
-3000	L1 to PE	0	Pass
+3000	L1 to PE	90	Pass
-3000	L1 to PE	90	Pass
+3000	L1 to PE	180	Pass
-3000	L1 to PE	180	Pass
+3000	L1 to PE	270	Pass
-3000	L1 to PE	270	Pass

16.3 Common Mode Surge (L2 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 3 A (Pass / Fail)
+3000	L2 to PE	0	Pass
-3000	L2 to PE	0	Pass
+3000	L2 to PE	90	Pass
-3000	L2 to PE	90	Pass
+3000	L2 to PE	180	Pass
-3000	L2 to PE	180	Pass
+3000	L2 to PE	270	Pass
-3000	L2 to PE	270	Pass

16.4 Common Mode Surge (L1, L2 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 3 A (Pass / Fail)
+3000	L1, L2 to PE	0	Pass
-3000	L1, L2 to PE	0	Pass
+3000	L1, L2 to PE	90	Pass
-3000	L1, L2 to PE	90	Pass
+3000	L1, L2 to PE	180	Pass
-3000	L1, L2 to PE	180	Pass
+3000	L1, L2 to PE	270	Pass
-3000	L1, L2 to PE	270	Pass

17 Electrostatic Discharge

The unit was tested with ±8.8 kV contact discharge and ±16 kV air discharge at the output VBUS, output GND, on-board, with 10 strikes for each condition. A test failure was defined as an interruption of output (latch-off) that needs operator intervention to recover, or a complete loss of function which is not recoverable.

17.1 Contact Discharge, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (On Board)	Test Result 5 V / 0 A	Test Result 5 V / 3 A	Test Result 20 V / 0 A	Test Result 20 V / 3 A
+8.8	Output VBUS	Pass	Pass	Pass	Pass
	Output GND	Pass	Pass	Pass	Pass
-8.8	Output VBUS	Pass	Pass	Pass	Pass
	Output GND	Pass	Pass	Pass	Pass

17.2 Air Discharge, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (On Board)	Test Result 5 V / 0 A	Test Result 5 V / 3 A	Test Result 20 V / 0 A	Test Result 20 V / 3 A
+16.5	Output VBUS	Pass	Pass	Pass	Pass
	Output GND	Pass	Pass	Pass	Pass
-16.5	Output VBUS	Pass	Pass	Pass	Pass
	Output GND	Pass	Pass	Pass	Pass

18 Revision History

Date	Author	Revision	Description & Changes	Reviewed
18-Jan-23	KR	1.0	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

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